Reducing Jitter in Nonuniform Sampling Drivers

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Outline

- Why nonuniform sampling?
- Influence of jitter
- Hardware performance before improvement
- The solution
- Improved Hardware performance
- Summary

Why Nonuniform Sampling?

Goal:

- Tackle Nyquist theorem for bandpass signals
- Enhance sampling efficiency

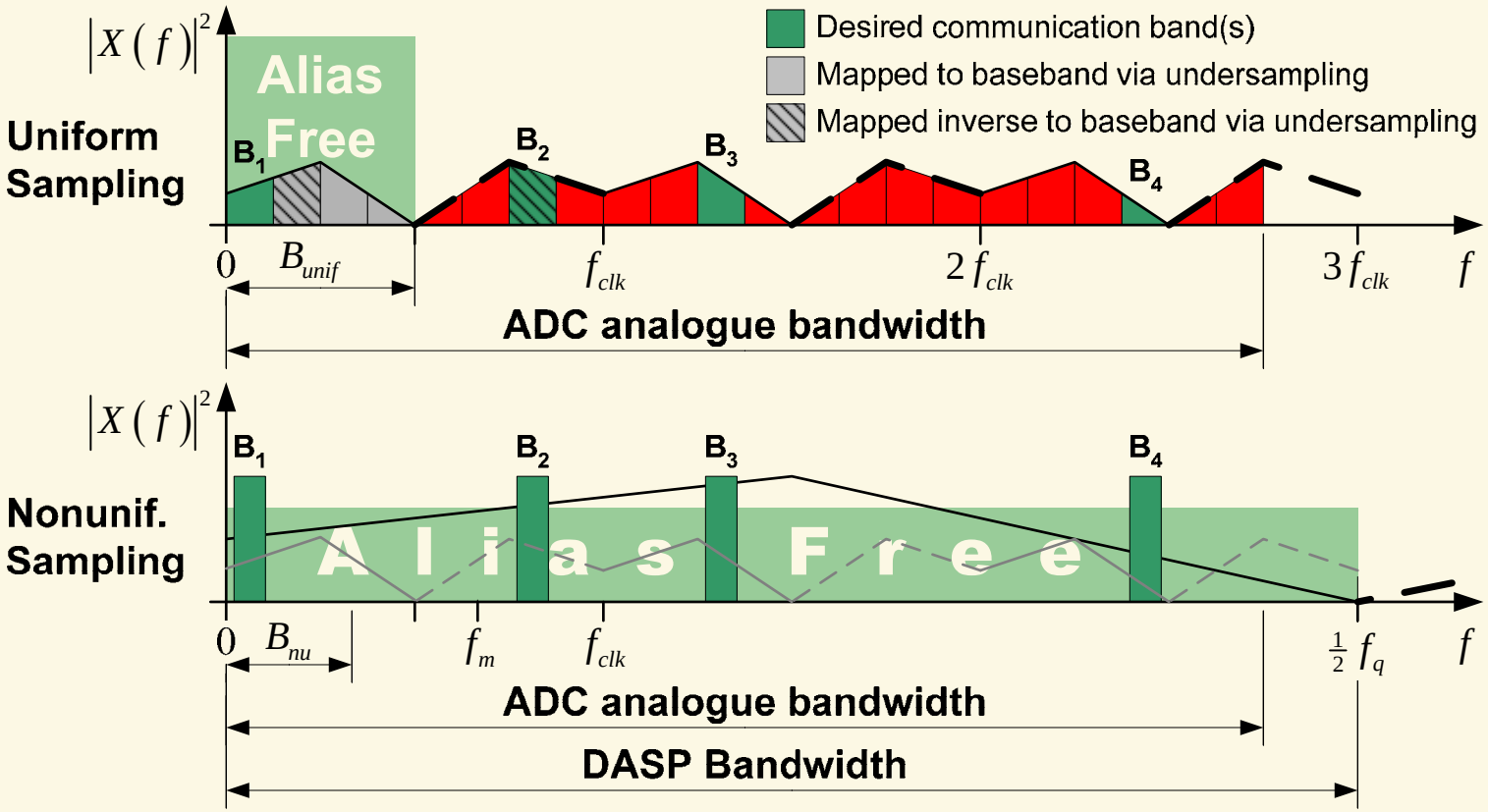
Advantages:

- Aliasing can be avoided
- Extreme *flexibility* choosing operational bands in Software Defined Radio (SDR) environments

Drawbacks:

- Increased processing complexity
- Suitable sampling schemes difficult to create (sampling driver (SD) needed)

Why Nonuniform Sampling? (II)



Influence of Jitter on System Performance

- Two main random error sources
  - Quantisation
  - Sampling instance jitter

$$SNR = 10\log_{10}\left(\frac{P_x}{P_q + P_{jitter}}\right)$$

- SNR due to *quantisation*

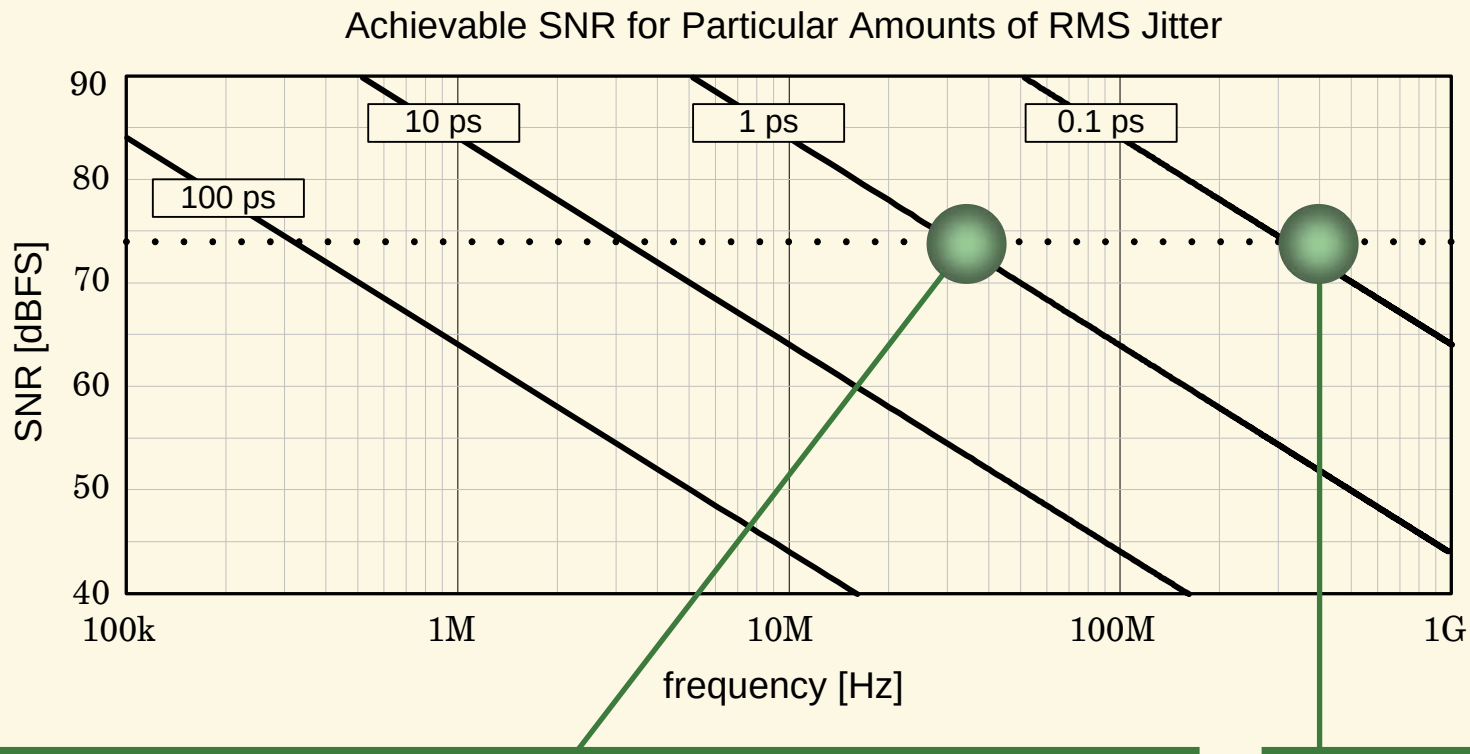
$$SNR_q \cong 1.76 + 6.02B$$

- SNR due to *jitter* (worst case approxim.)[1]

$$SNR_j \cong 10\log_{10}\left(\frac{1}{(2\pi f_{max})^2 \sigma_j^2}\right)$$

[1] J. Horn, *Clock jitter and ADCs.* Jun. 9, 2000. http://archive.chipcenter.com/eexpert/jhorn/jhorn026.html

Influence of Jitter on System Performance (II)



Achievable maximum due to clock source

Vision

Influence of Jitter on System Performance (III)

- Decreases system bandwidth[2]

$$f_{\varepsilon}(t) * x_s(t) \rightarrow \Phi_{\varepsilon}(f) X_s(f)$$

$$\Phi_{\varepsilon}(f) \cong 1 - 2\pi^2 f^2 \sigma_j^2$$

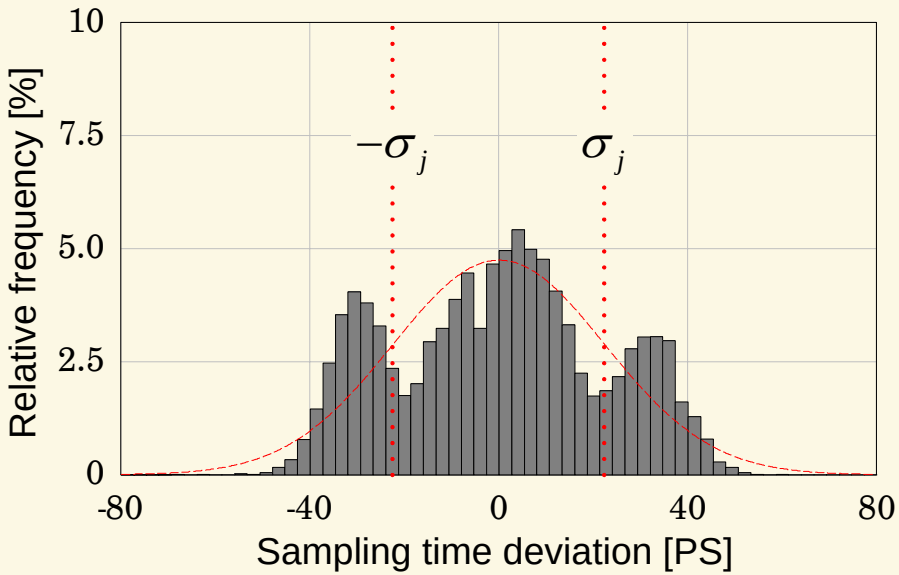
- Use estimated variance to correct frequency response

$$X_s(f) \cong \frac{\hat{X}(f)}{1 - 2\pi^2 f^2 \sigma_j^2}$$

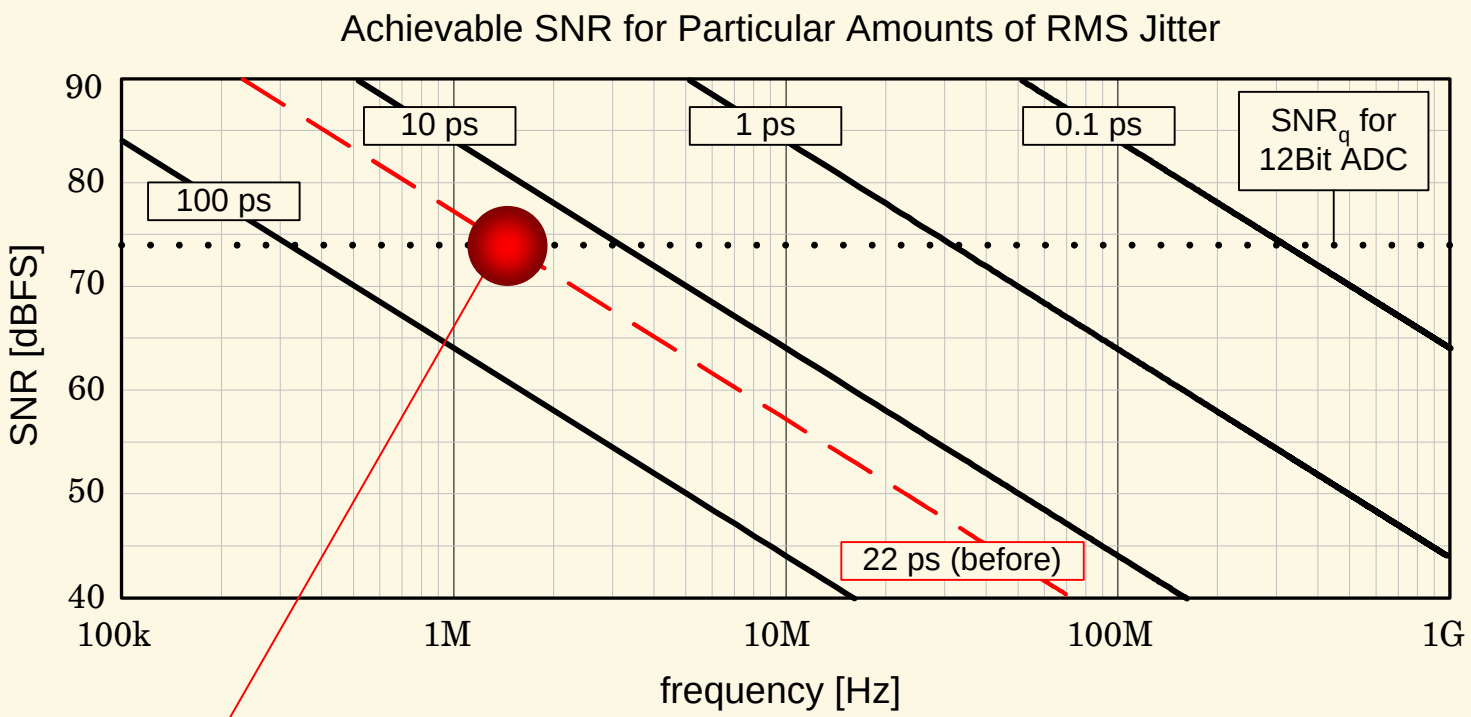
[2] A. Tarczynski and N. Allay, “Spectral analysis of randomly sampled signals: suppression of aliasing and sampler jitter,” *Signal Processing, IEEE Transactions on*, vol. 52, no. 12, pp. 3324-3334, 2004.

Performance before Improvement

- Measured jitter: *22 ps* RMS, multimodal distribution (approximated unimodally)

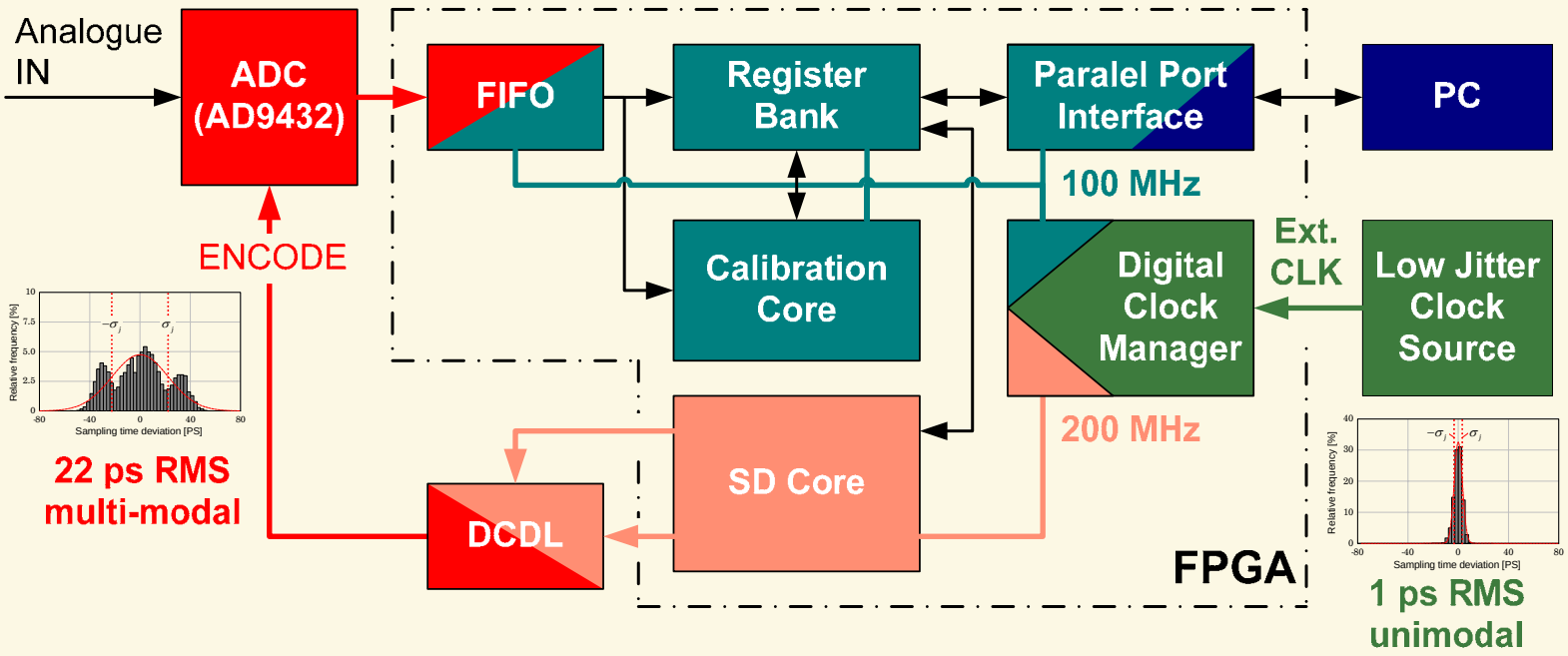


Performance before Improvement (2)

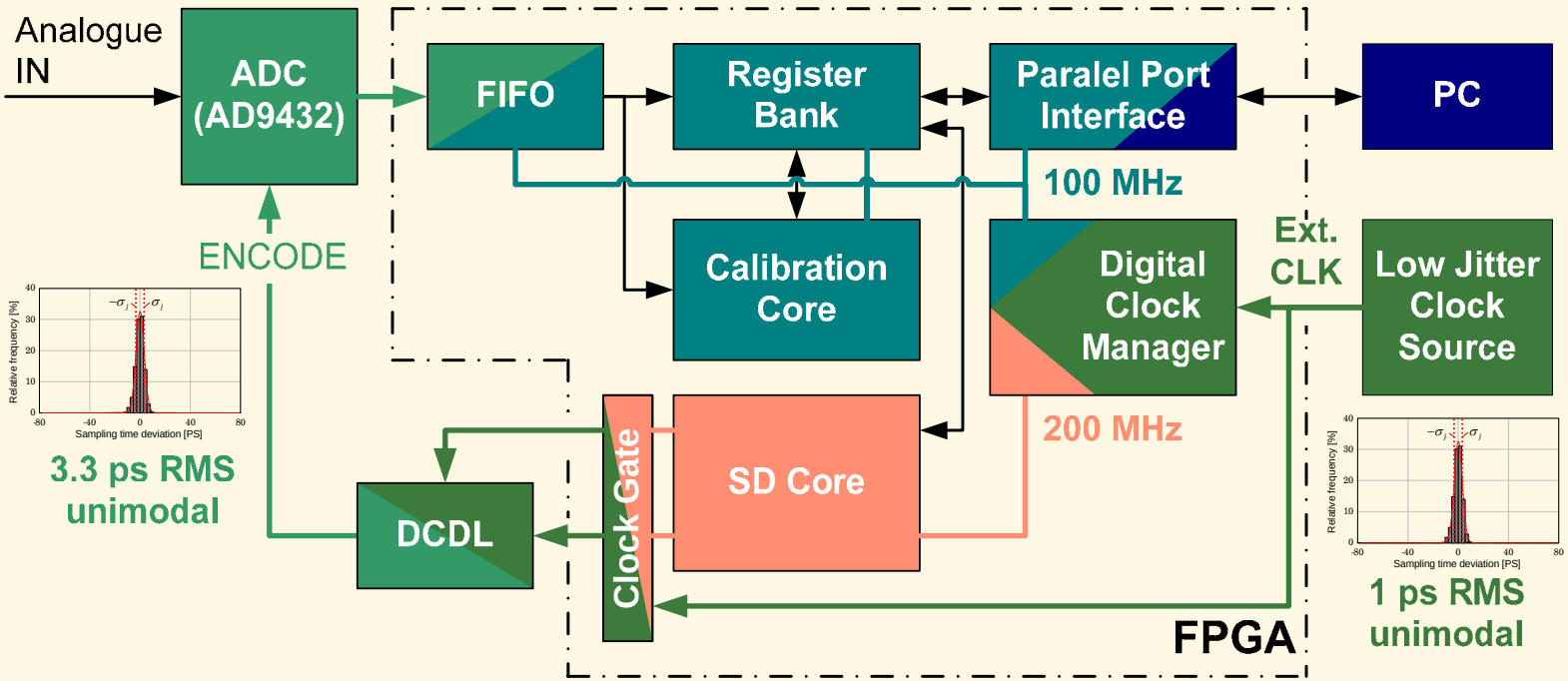


Poor full SNR operational range (DC to 1.5 MHz)

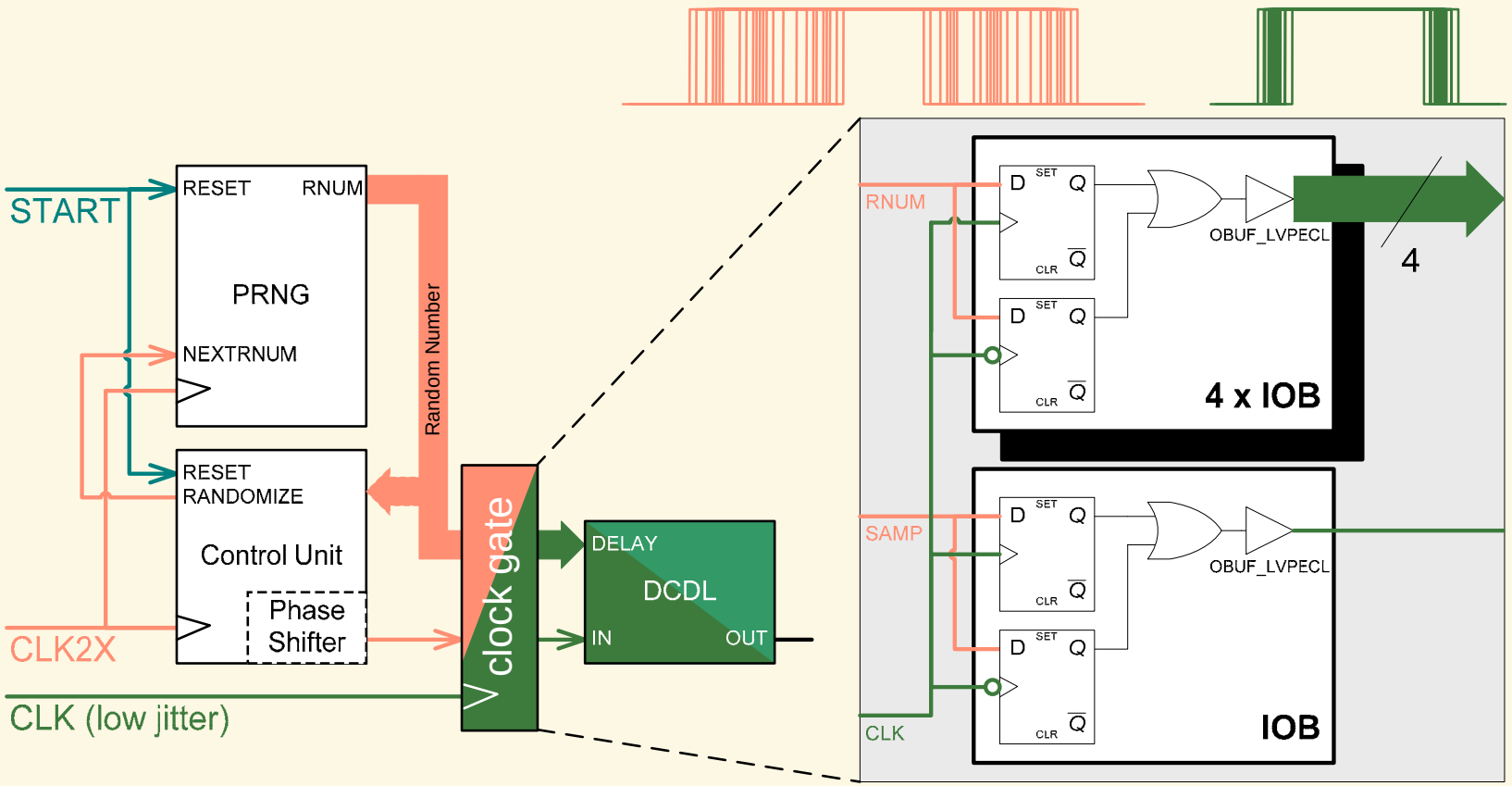
The Problem


Analogue IN
ADC (AD9432)
ENCODE
FIFO
Register Bank
Paralel Port Interface
PC
100 MHz
Calibration Core
Digital Clock Manager
Ext. CLK
Low Jitter Clock Source
200 MHz
SD Core
DCDL
FPGA
Relative frequency [%]
Sampling time deviation [PS]
22 ps RMS multi-modal
1 ps RMS unimodal

The Solution

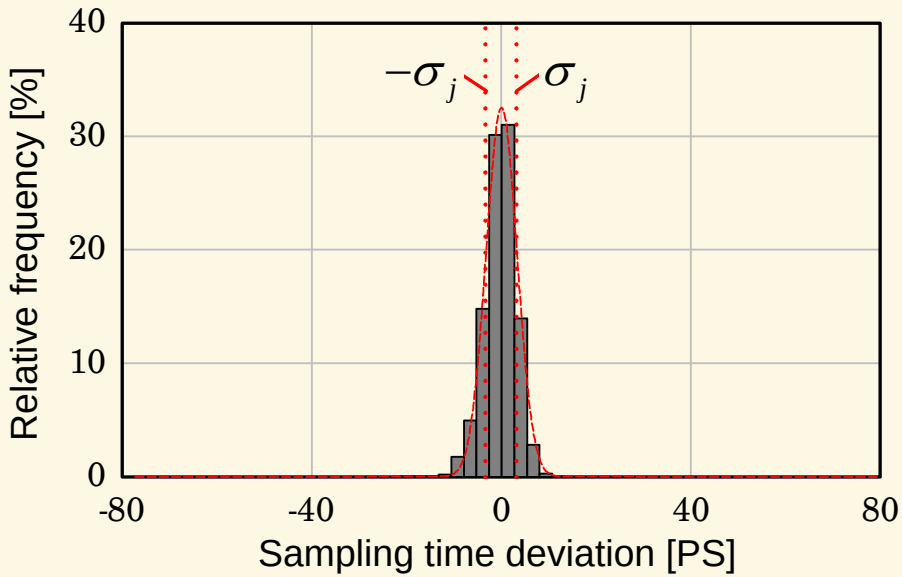


The Solution (II)

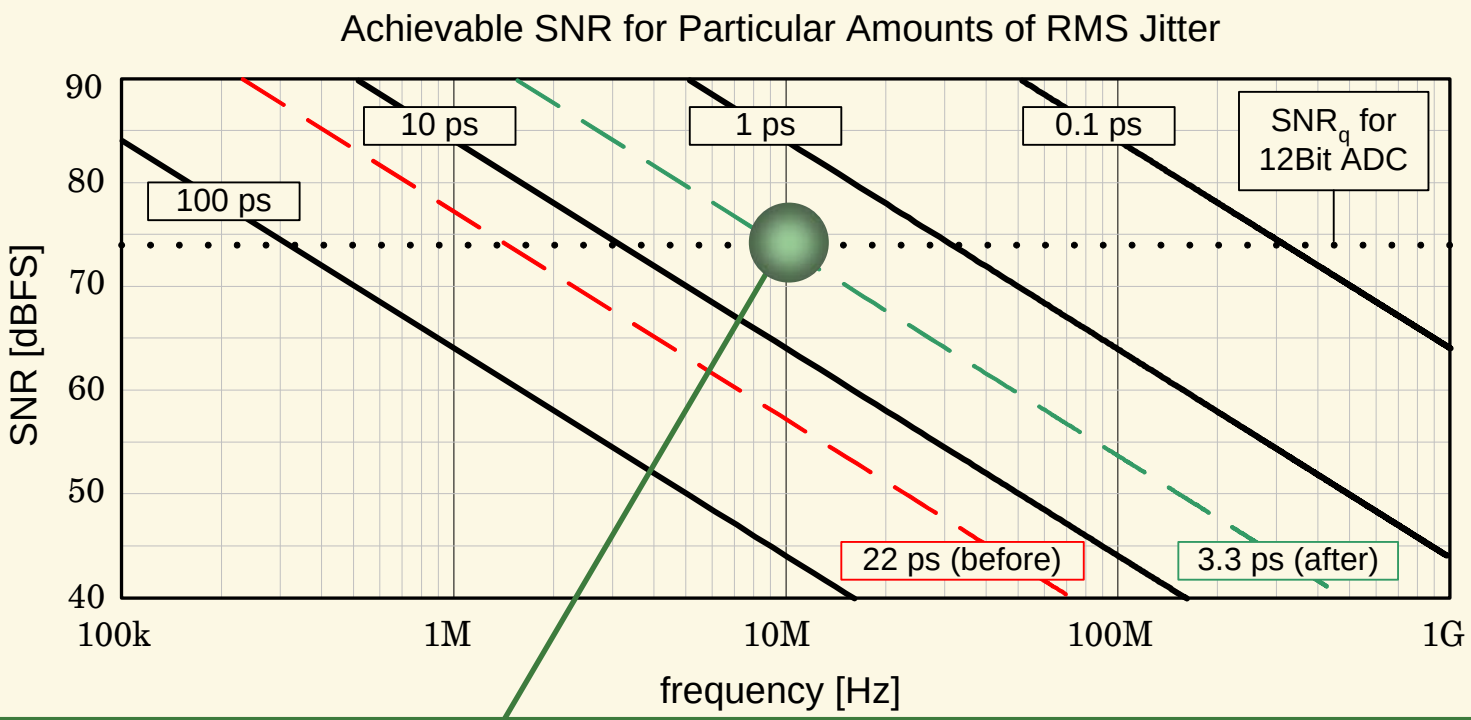


Performance after Improvement

- Measured jitter: *3.3 ps* RMS, unimodal Gaussian distribution



Performance after Improvement (II)



Enhanced full SNR operational range (DC to 10 MHz)

Summary

- *Clock gating* enables effective S&H clock jitter reduction
- Proposed method robust and applicable to variety of SD designs (static timing analysis)
- RMS jitter reduced by an order of magnitude!
- Still room for improvement (PCB layout)

Questions?

- Current state of the art oscillators feature *1 ps* RMS jitter! Getting below 1 ps represents a challenge.

- Optical clock generators may represent an opportunity to supply lower jitter clock sources (Prof. José Azaña)