Scalable Counter Architecture for a Preloadable 1GHz@0.6µm/5V Pre-scaler in TSPC

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Outline

- Motivation
- DTSPC circuit style
- SD adder architecture
- Pre-scaler circuit design
- Optimizations
- Results
Motivation

- Architecture of a pre-scaler circuit is most often fixed to a specific divider ratio
- For a variable divider ratio adder functionality is needed
- To achieve high clocking rates dynamic circuit technology is utilized
- Non redundant adder structures like RCA, CSUM, ... can't fulfill the requirements of one clock cycle per operation (word length dependent calculation time)
- Redundant adder basic structures exceed the size of a single cell implementation? multiple clock cycles needed for a word length independent addition

Requirements

- One clock cycle redundant adder circuit
- Easily determinable reload event (zero crossing state)
Differential True Single Phase Clock circuit style

- based on the True Single Phase Clock (TSPC) circuit technology
- Generates both output signals, inverted and non-inverted, without different P/N2-block style
- Robust cell behavior
- Cells can be cascaded
DTSPC Signed-Digit (SD) adder standard cell
DTSPC Signed-Digit adder standard cell (2)

N-Block

N2-Block

N-Block

N2-Block

clk_buf_tree

clk_buf_tree

clk_buf_tree
DTSPC Signed-Digit adder standard-cell (3)

Austria Micro Systems
0.6µm technology
transistor count: 121
area: 38 x 185 µm
speed: 1.1 GHz
Pre-scaler Circuit Design

- Utilization of a DTSPC SD-adder standard cell
- Only with SD-number system one value (0) has a non-redundant representation
- Addition of the increment to a negative pre-load/counter value reduces pseudo overflow
- Zero crossing determined by TSPC-OR logic register
- Scalable bit width
- 1GHz@0.6µm/5V
- Optimization of adder cells in different digit positions possible

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![Pre-scaler Circuit Diagram](image-url)
Pre-scaler Optimization

SD-Incrementer

<table>
<thead>
<tr>
<th></th>
<th>2^3</th>
<th>2^2</th>
<th>2^1</th>
<th>2^0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sn</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Dn</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

SD-Decrementer

<table>
<thead>
<tr>
<th></th>
<th>2^3</th>
<th>2^2</th>
<th>2^1</th>
<th>2^0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sn</td>
<td>0</td>
<td>0</td>
<td>-1</td>
<td>0</td>
</tr>
<tr>
<td>Dn</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

3 different cells

4 different cells

used operand digits
Experimental Results

Post-layout simulation with extracted cap and resistors under typical conditions

<table>
<thead>
<tr>
<th>Design</th>
<th>Technology @ power supply</th>
<th>Area (10^3 mm^2)</th>
<th>Speed (GHz)</th>
<th>Power (µW/MHz)</th>
<th>Pre-scaler Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chang</td>
<td>0.8 @ 5</td>
<td>13.7</td>
<td>1.22</td>
<td>20.9</td>
<td>128/129</td>
</tr>
<tr>
<td>Soares</td>
<td>0.8 @ 5</td>
<td>12.6</td>
<td>1.59</td>
<td>8</td>
<td>128/129</td>
</tr>
<tr>
<td>Sd5</td>
<td>0.6 @ 5</td>
<td>41.6</td>
<td>1.07</td>
<td>365.5</td>
<td>52 – 31</td>
</tr>
<tr>
<td>Sd8</td>
<td>0.6 @ 5</td>
<td>62.1</td>
<td>1.01</td>
<td>597.3</td>
<td>52 – 255</td>
</tr>
</tbody>
</table>

Only minimal speed reduction by growing word length
High power and area consumption make this architecture not suitable for all applications
Gives freedom to choose divider ratio in-circuit
Conclusion

? With DTSPC circuit style highly complex cell functions can be implemented
? DTSPC delivers both output signal levels in parallel, no additional circuits and delays needed to generate inverted and non-inverted signals
? SD number system reduces necessary effort for determination of reload event
? Redundant binary number representation gives a wide range of divider ratios with only a small number of digit positions