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Scalable Counter Architecture for a Pre-loadable $1GHz@0.6\mu m/5V$ Pre-scaler in TSPC

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ABSTRACT

In this paper we describe an approach for using the true single phase clock (TSPC) circuit style for the implementation of a scalable, pre-loadable pre-scaler. By utilization of a signed digit (SD) based redundant adder cell the execution of the necessary addition operation can be performed in only one clock cycle, independent from the length of the applied operators. The development process for this SD-adder cell by reorganization and partitioning of the necessary logic in connection with an enhancement of the TSPC circuit style will be discussed. The determination of the zero-crossing is also as far as possible independent from the word length by deployment of a TSPC OR-cell.

Furthermore, a reference implementation of a 8-digit pre-scaler circuit operating at 1GHz with a 5V power supply in a $0.6\mu m$ AMS CMOS process will be presented.

The goal of this paper is to develop a strategy for the implementation of pre-scaler circuits based on redundant arithmetic, which can operate at high frequencies. The comparison with the results of other implementations illustrate the advantages of our approach.

1. INTRODUCTION

High-speed frequency divider circuits are necessary for the implementation of circuits like phase-locked loop (PLL), which are utilized in transceiver devices. Unfortunately, this pre-scaler or frequency divider circuits, presented in previous works like [1],[2], were build only with fixed or bounded operation modes. The limitation is indispensable, because a generic architecture with conventional adder structures can't fulfill the timing requirements.

In this paper the architecture of a scalable pre-scaler with runtime configurable divider ratio using a $0.6\mu m$ CMOS technology is described. In section 2 the principles of the utilized technologies will be shortly discussed and analyzed. A detailed explanation of the reorganization and partition of the fundamental SD-adder are presented in section 3. The pre-scaler architecture is presented in section 4. Our experimental results and the comparisons with other existing solutions are reviewed in section 5. Section 6 is dedicated to the conclusion.

1.1. Previous approaches

A majority of implementations of a pre-scaler is based on TSPC circuits like shown in [1][2]. Commonly the implementation of a pre-scaler is based on a simple combination of register cells with only a small amount of combinatoric logic. That means, the state machine for the divider is mainly implemented by the wiring of the registers. Through the reduction of the necessary combinatorial logic between the registers, the circuit can operate at nearly the value of the register toggle frequency. The disadvantage of such a solution is the fixed divider ratio by the architecture so that for each new ratio the circuit has to be redesigned. Mostly, no more than two different ratios are implemented by one pre-scaler circuit.

2. FUNDAMENTALS

In the following section a short introduction into the utilized circuit technology and arithmetic family will be given.

2.1. True Single Phase Clock circuit style

True Single Phase Clock (TSPC) technique first presented in [3] can be implemented as shown in Fig. 1. The logic function is implemented in the n-logic block (the same is possible for the p-block with decreased speed) by a custom network of NMOS transistors. These are limited by technology and speed requirements with respect to the number of transistors in series. There are also some minor limitations with respect to the number of parallel transistors. Due to the even number of inverter stages only noninverting functions like and and or are possible in one dynamic block. This results in the requirement for a modified net-list which has signal inverters at the input or/and the output of the whole circuit only. The modification of the net-list, mainly the separate inspection of the net-list for each output signal, usually results in a higher gate count. This is partly compensated by a following search for collapsing terms in the resulting net-list trees.

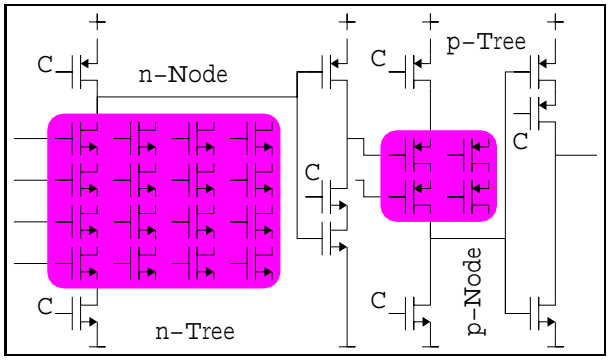

Figure 1: TSPC circuit

2.2. Differential True Single Phase Clock circuit style

One possible solution to prevent this undesirable increase of the net-list is the use of Differential True Single Phase Clock logic.

It is similar to Differential NORA logic (DNORA) [4] but like TSPC it lacks the feedback circuit found in NORA. A DTSPC-cell consists of two TSPC cells with complementary logic networks to generate differential output signals which eliminates the above mentioned preparation of the net-list. An AND2/NAND2 example is shown in Fig. 2. On the other hand, the number of interconnections and, consequently, cell area increase as well for this kind of circuit style.

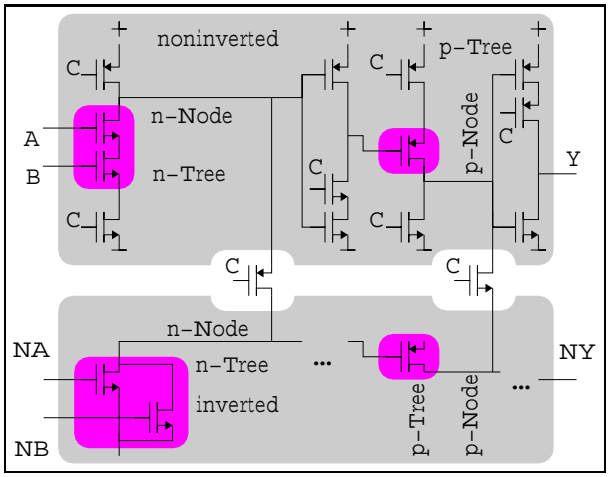

Figure 2: DTSPC circuit

2.3. Redundant adder architectures

Conventional binary adder structures like ripple carry adders (RCA) or speed improved architectures in a standard CMOS technology have a word-length dependent operation-time. By implementation of such an architecture with a dynamic logic style this results into a word-length dependent latency. This behavior can only be tolerated in a pipelined environment. For the implementation of non-pipelined architectures like counters we have to utilize an architecture for the arithmetic with word-length in-depended characteristic. Besides the carry-save (CS) arithmetic the signed-digit (SD) approach, utilizing a number representation as shown in [5], can fulfill our requirements. In both architectures an operand digit has only impact on the next two higher order digits in the result of the addition contrary to the influence in a binary adder. Unfortunately, the implementation of a SD-adder can't be efficiently realized with standard binary adder cells, like the CS-approach.

The smallest realization in a standard CMOS technology of a SD-adder (Fig. 3) was first presented in [6].

A simple implementation of this SD adder functionality with TSPC technique for the 11 necessary logic cells also doesn't meet our requirements of one clock cycle per calculation. Furthermore, through the relative small amount of logic in each of this cells, we don't exploit the possibilities of a TSPC cell.

3. SD CELL DESIGN

As first step in the design of the SD-adder cell we have to factor out the utilized logic in Fig. 4 for the adder with the circuit from

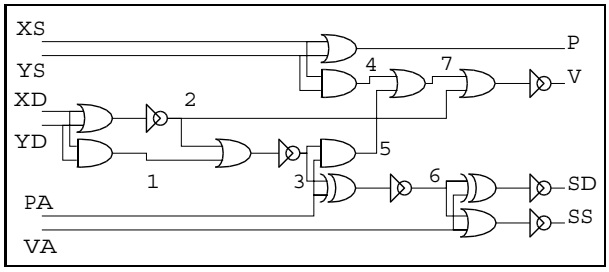

Figure 3: SD adder by Takagi [6]

Fig. 3. By this, we can achieve that each output signal of the SD-adder cell is generated only from the input signals. The formerly presented dependency from signals of the lower blocks is removed by duplication of the necessary logic.

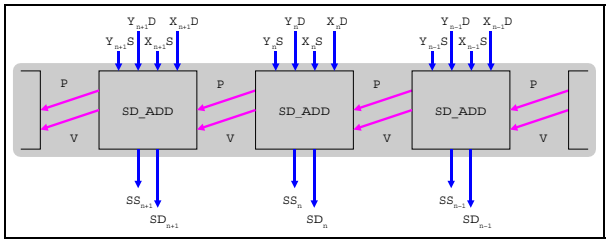

Figure 4: SD adder row

This expanded SD-adder circuit is a condition for the strived goal of one clock cycle per calculation. The increase of cell area by the doubled circuit structures will be limited through the restriction of the TSPC logic implementation in only one tree of transistors.

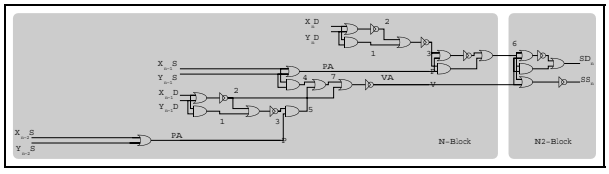

Figure 5: Expanded SD adder circuit

Due to the huge amount of logic in one adder cell, we also have to partition the circuit as shown in Fig. 5 for the tree implementation on both basic blocks of a TSPC cell, the fast n-block and the somewhat slower n2-block according to [3]. With this step two new internal signals s_6 and s_vav between the both tree partitions will be introduced. Next we have to move the internal negation functions in both partitions to the input pins as shown in Fig. 6 for the s_6 signal n-tree.

After this step, each block requires noninverted and inverted input signals. This complementary signals can easily be generated by utilizing the DTSPC circuit style for the whole cell. Each block has therefore to be replicated by its differential representation. The resulting circuit for a full functional SD-adder cell in DTSPC technique is shown in Fig. 7.

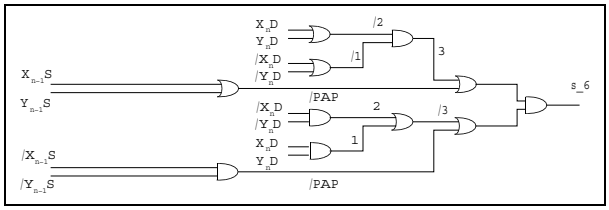

Figure 6: s_6 signal n-tree without internal negations

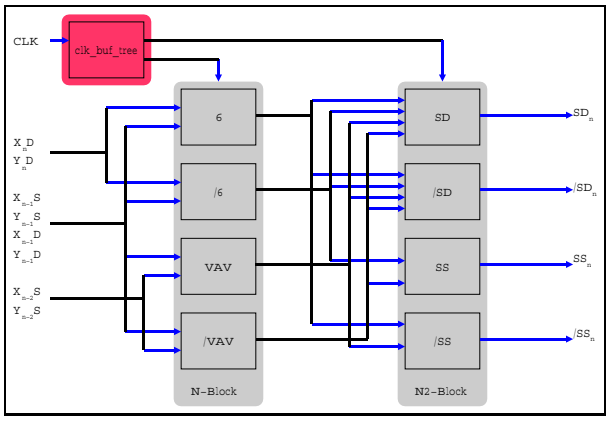

Figure 7: DTSPC circuit of the SD-adder cell

As part of a library for a dynamic logic synthesis design-flow [7] this SD-adder has been implemented in a $0.6\mu m$ AMS technology as a standard cell shown in Fig. 8. According to the geometry definition in the CUB-technology for standard cells the sd-adder cell has a size of $38\mu m * 185\mu m$. The relative flat geometry leads to an increased non optimal wire length for cell internal connections. Furthermore, the overhead of NMOS transistors, typically for dynamic circuit techniques like TSPC, is easily recognizable.

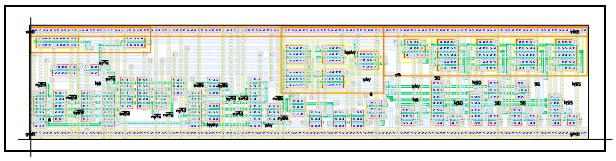

Figure 8: Layout of the $0.6\mu m$ AMS SD-adder standard cell in DTSPC

This standard cell library was designed to operate at clock frequency of $1GHz@5V$ in pipelined designs like [8]. To simplify the utilization of the TSPC-circuits as standard cells for each library cell a carefully implementation of the cell internal clock buffer structure has been done to equalize the fan-in of the clock signal and the internal clock skew.

4. PRE-SCALER CIRCUIT DESIGN

Based on the previously introduced SD-adder cell, the development of a configurable high speed counter circuit has been done. The pre-load value and also the counting direction is choseable at runtime. Due to the internal SD number representation of the state vector the counting range is nearly doubled with respect to a binary implementation. To implement the pre-scaler circuit shown in Fig. 9, the easily detectable zero crossing state of the SD-counter was been utilized to reload the counter circuit with the divider value and generate the pre-scaler output signal. Unfortunately, due to this, the signal generation of our pre-scaler has only a non-symmetric output waveform. The zero crossing is the only state of the counter which has exactly one representation in the SD-digit counter vector. Each other counter state can have, due to the redundant behavior of the SD-adder, more than one different representation in the SD-digit counter vector. Through the utilized SD-arithmetic the resulting counter is nearly word-length independent. Only the circuit for the determination of zero crossing becomes word-length depending with higher word-length. For the commonly utilized word-length values the TSPC implementation of the necessary OR-gate, an array of parallel connected NMOS transistors, is characterized by a similar timing behavior.

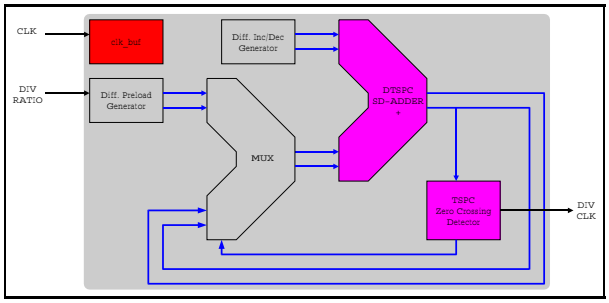

Figure 9: SD Pre-scaler

A further improvement of the pre-scaler circuit is the reduction of the SD-adder block to a smaller SD-incrementer. By this simplification the implementation effort for internal SD-adder cells can be reduced by nearly the half. Through this decrease of necessary logic the realization of the incrementer cells can be repartitioned to prevent a logic implementation with serialized NMOS transistors in the slower N2-blocks of the adder cell. Unfortunately, three different cells are necessary to realize the functionality derived from the initial adder cell with partially fixed inputs.

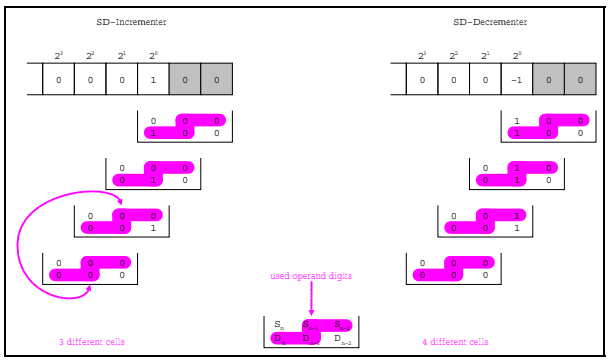

Figure 10: Comparison of SD-Incrementer and Decrementer

An SD-decrementer implementation is unfavorable due to the increased mobility of the significant digits in the counter vector during the operation in the positive value range and also through the higher effort for the implementation of a SD-decrementer against the incrementer version shown in Fig. 10.

5. EXPERIMENTAL RESULTS

To verify our approach, two different implementations have been realized. At first, a pre-scaler with an internal 5 digit counter vector and also an 8 digit wide implementation have been investigated.

Fig. 11 shows the resulting waveform for the 8 digit implementation at an operating frequency of $1GHz$ for a divider ratio of $5:1$ simulated at typical conditions. Furthermore, in the waveform the offset between the global clock signal n_sig and the standard cell's internal locally buffered clock signal c_pre can be seen. As mentioned above, this offset has been equalized during the library development for the whole set of cells.

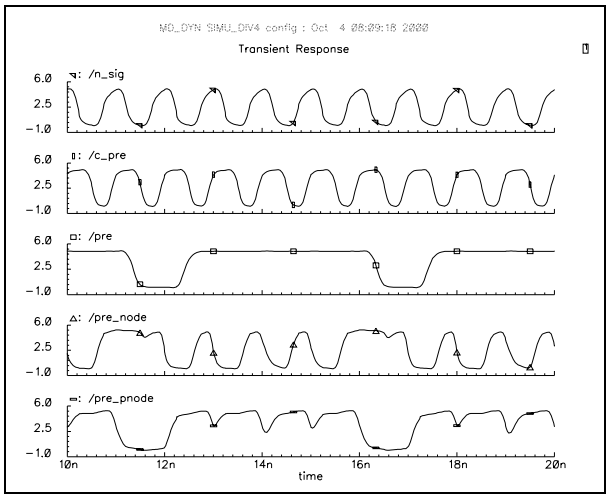

Figure 11: Back-annotation of the 8digit pre-scaler with 5:1 divider ratio

Our results compared with a few references in Tab. 1 have been obtained by simulation of the back-annotated layouts. With our 8 digit wide implementation a similar divider ratio like on the two fixed dual modulus 128/129 pre-scalers are possible.

Design	Technology @ power supply $(\mu m @ V)$	Area $(10^{-3} mm^2)$	Speed (GHz)	Power $(\frac{\mu W}{MHz})$	Pre-scaler Ratio
[1]	0.8@5	$13.7^{(*)}$	1.22	20.9	128/129 dual mode fixed
[2]	0.8@5	12.6	1.59	8.0	128/129 dual mode fixed
sd5	0.6@5	41.6	1.07	365.5	selectable in range 2-31
sd8	0.6@5	62.1	1.01	597.3	selectable in range 2-255

Table 1: Comparison of Area, Speed and Power-consumption Results

$(*)$ only the divide-by-4/5 and the divide-by-32 counters are considered

The analysis of this comparison demonstrates the overhead, which has to be considered for the scalability and adjustability of a pre-scaler device. The increase of the adjustable implementation concerning the area is relatively small. Unfortunately, the drastically increased power consumption of our proposed approach limits the field of application to mostly stationary units. This increase is mainly justified by the doubled implementation amount in the DTSPC cells. Furthermore, the fact of scalability of our architecture is been supported by the small difference of the measured results.

6. CONCLUSIONS

A scalable high-speed runtime adjustable pre-scaler architecture was developed in a $0.6\mu m$ CMOS process. The results of our implementation demonstrate the suitability of the proposed approach. A further improvement of the results has been achieved by the migration from a general SD-adder representation to an adapted SD-incrementer implementation. The utilized DTSPC circuit technique together with the redundant arithmetic enables the necessary speedup for the implementation of complex systems like the presented adjustable pre-scaler architectures to operate above the $1GHz$-border.

7. REFERENCES

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