Precise Indoor Localization with Low-Cost Field-Programmable Gate Arrays

Enrico Heinrich and Ralf Joost and Marian Lüder and Ralf Salomon
Faculty of Computer Science and Electrical Engineering
University of Rostock
18051 Rostock, Germany
e-mail: {enrico.heinrich,ralf.joost,marian.lueder,ralf.salomon}@uni-rostock.de

***Abstract*—This paper explores to what extent an abstract model of the barn owl auditory system can be utilized as the core of a digital indoor localization system. A first prototype has been implemented on a low-cost Altera Cyclone II field-programmable gate array. With a system clock of 85 MHz, this prototype yields a resolution of about 0.02 ns for frequencies ranging from 11 kHz to up to 300 MHz. The achieved time resolution equals a spatial resolution of about 1 mm.**

I. Introduction

From a technical point of view, the barn owl has an astonishing localization system [1]: it allows the barn owl to locate its prey with an accuracy of about 2°, which is much better than the processing speed of *single neuron* would allow; its remarkable localization performance is due to the computations of the *entire set* of nerve cells, which are furthermore interconnected in a very "smart" way.

The barn owl auditory system is organized as follows (see, also, Fig. 1): The *nucleus laminaris* consists of a large number of asynchronously operating coincidence detectors, which are connected to two anti-parallel axonal delay lines. At their opposing ends, each axonal delay line connects to one of the two ears. Every sound signal arrives at the auditory system via two different paths, i.e., through the left and through the right ear. For obvious physical reasons, a neuron observers a coincidence, i.e., a zero phase shift between the two signals, only if the total delays through both paths are equivalent. As a consequence, every neuron preferably responds to its own individual angle under which the sound source appears.

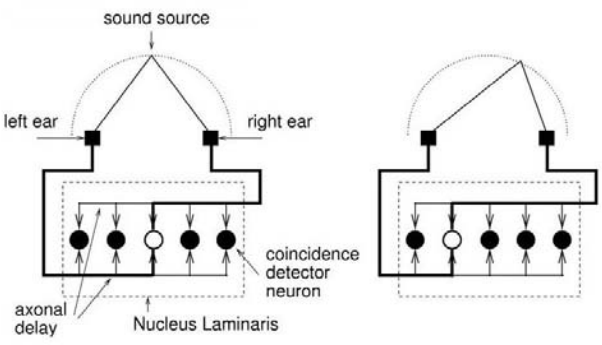

Fig. 1. The auditory localization system of the barn owl [1].

From a computational point of view, it is important to note that the barn owl generates the internal time delays by means of passive axonal structures. These *length-dependent* time delays are only *fractions* of the delays fast-processing neurons exhibit. As a result, the barn owl auditory system achieves a spatial resolution that is better than the processing speed of the neurons would allow.

Since it has not been done by previous research, this paper explores to what extent an abstract model of the barn owl auditory system can be utilized in a technical application. To this end, Section II presents an architecture that is called X-ORCA and that consist of only digital processing elements, such as logic gates and counters. Like the role model, the X-ORCA architecture relies on two key features: (1) it employs a large number of asynchronously processing elements each of which models a coincidence detector module as an XOR gate and a counter, and (2) it generates the desired signal delays by the regular on-chip wires on which the signals travel with about 2/3 of the speed of light. This combination might seem a little surprising to some readers. However, previous research [2] has already shown that this approach is indeed physically working in particular contents.

If implementing the X-ORCA architecture on a "regular" processor, such as a micro controller or a signal processor, most of the inherent parallelism would get lost; all the ongoing activity would be synchronized with the internal system clock. For an asynchronously operating architecture, such as X-ORCA, a field-programmable gate array (FPGA) would be a better implementation platform. An FPGA is a hardware device, which consists of about 5,000 to 500,000 logic elements. By using a C-like hardware description language, such as VHDL [3] or Verilog [4], these logic elements can be configured and interconnected at the programmer's desire. This approach allows for the conservation of the inherent parallelism on the hardware level. Therefore, a first prototype has been implemented on an Altera Cyclone II field-programmable gate array (FPGA) [5]. Section III provides all the implementation details as well as the experimental setup.

The results of the practical experiments are summarized in Section IV, and show that already the first prototype yields a resolution of about 20 ps. Finally, Section V concludes this paper with a brief discussion.

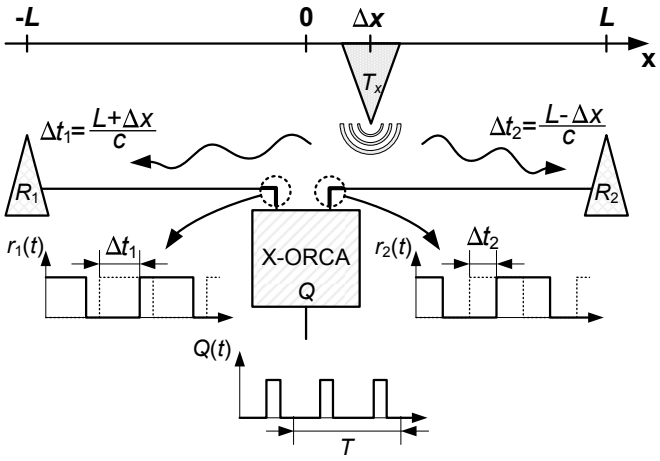

Fig. 2. X-ORCA assumes a standard, one-dimensional setup in which the time difference $\Delta t = t_1 - t_2 = 2\Delta x/c$ is a result of the transmitter's off-center position Δx. It indirectly determines $\Delta t = \Delta\varphi/(2\pi f)$ by estimating the phase shift $\Delta\varphi$ between the two incoming signals $r_1(t)$ and $r_2(t)$.

II. The X-ORCA Localization System

This section presents the X-ORCA architecture in three parts. The first parts starts off by clarifying the physical setup and all the assumptions made in this paper. The second part explains X-ORCA's core principles. In so doing, it makes a few assumptions that might *seem* practically implausible for some readers. However, the third part elaborates on how the X-ORCA architecture and the assumptions made in the second part can be fully realized on standard circuits.

A. Physical Setup and Preliminaries

Since the aim of a single X-ORCA instance is to determine the phase shift $\Delta\varphi$ between two incoming signals, it can be used as the core of a one-dimensional localization system. It thus adopts a standard setup (see, also, Fig. 2) in which a transmitter T emits a signal $s(t) = A\sin(2\pi f(t - t_0))$ with frequency f, amplitude A, and time offset t_0. Since this signal travels with the speed of light $c \approx 3 \cdot 10^8$ m/s, it arrives at the receivers R_1 and R_2 after some delays $\Delta t_1 = (L + \Delta x)/c$ and $\Delta t_2 = (L - \Delta x)/c$.

Both receivers employ an amplifier and a Schmitt trigger, and thus feed the X-ORCA system with the two rectangular signals $r_1(t - t_0)$ and $r_2(t - t_0)$ that both have frequency f. By estimating the phase shift $\Delta\varphi$ between these two signals $r_1(t - t_0)$ and $r_2(t - t_0)$, X-ORCA then determines the time difference $\Delta t = t_1 - t_2 = \Delta\varphi/(2\pi f)$, in order to arrive at the transmitter's off-center position $\Delta x = \Delta t c/2$.

It might be, though, that both the physical setup and the X-ORCA system have further internal delays, such as switches, cables of different lengths, repeaters, and further logical gates. However, these internal delays are all omitted, since they can be easily eliminated in a proper calibration process.

In a real-world, three-dimensional scenario, a localization system has to provide three coordinates $x_1, \ldots, x_3$. To this end, a system has to implement three X-ORCA instances, which might (but not necessarily have to) share three receivers, resulting in four receivers and three independent X-ORCA implementations.

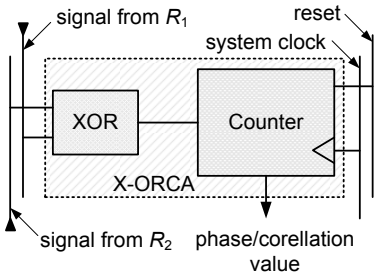

Fig. 3. An X-ORCA phase detector consists of a logical XOR (or any other suitable binary logic function), which "mixes" the two input signals s_1 and s_2, and an additional counter to actually determine the phase shift $\Delta\varphi$.

B. The System Core

Essentially, the X-ORCA core consists of a large number of independently operating phase detectors. Each of these phase detectors models the core features of a coincidence detector neuron of barn owl's *nucleus laminaris*. One of these phase detectors is illustrated in Fig. 3. It consists of a logical XOR and a counter. The XOR "mixes" the two input signals s_1 and s_2, and yields a logical 1 or a logical 0 on whether the two signals differ or not. In other words, the degree of how both signals differ from each other corresponds to the phase shift $\Delta\varphi$, and is represented as the proportion of logical 1's per time unit. This proportion is evaluated by the counter that is attached to the XOR gate.

For example, let us assume an input signal with a frequency of f=100 MHz and a phase shift of $\Delta\varphi$=$\pi/4$=45°. Then, if the counter is clocked at a rate of 10 GHz over a signal's period T=1/(100 MHz)=10 ns, the counter will assume a value of v=25.

At this point, three practical remarks should be made: (1) The XOR gate has been chosen for pure educational purposes; any other suitable binary logic function, such as AND, NAND, OR, and NOR, could have been chosen as well. (2) A counter clock rate of 10 GHz is quite unrealistic for technical reasons, but Subsection II-C shows how such clock rates can be virtually achieved. (3) A result of a phase shift $\Delta\varphi$=$\pi/4$=45°, for example, is intrinsically ambiguous, since the system cannot differ between p=$\pi/4$=45° and p=$-\pi/4$=$-45°$.

In order to solve the ambiguity of a single phase detector, X-ORCA simply employs more than just one. Figure 4 shows that X-ORCA places all phase detectors along two reciprocal (anti-parallel) "delay" wires w_1 and w_2 on which the two signals $r_1(t)$ and $r_2(t)$ travel with approximately two third of the speed of light $c_w \approx 2/3c$. Because the two wires w_1 and w_2 are *reciprocal*, all phase detectors have different internal delays τ_i which always add to the external delay $\Delta t = 2\Delta x/c$ that is due to the transmitter's off-center position Δx. As a consequence, each phase detector i observes an effective time delay $\Delta t + \tau_i$ and thus a phase shift $\Delta\varphi_i = 2\pi f(\Delta t + \tau_i)$.

Further post-processing stages become particularly easy, if

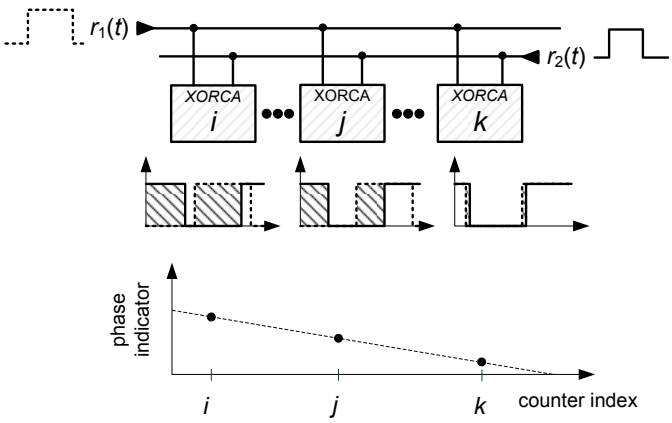

Fig. 4. X-ORCA places all phase detectors along two reciprocal (anti-parallel) "delay" wires w_1 and w_2 on which the two signals $r_1(t)$ and $r_2(t)$ travel with approximately two third of the speed of light $c_w \approx 2/3c$. Because the two wires w_1 and w_2 are *reciprocal*, all phase detectors have different internal delays τ_i.

the internal delays $\tau_i^{\max} - \tau_i^{\min} = T = 1/f$ span the entire range of a period T of the localization signal $s(t)$. For a first estimate of the transmitter's off-center position Δx it would suffice to determine the phase detector i that has the smallest counter value $v_i^{\min} = \min\{v_i\}$; only those phase detectors i have a counter value close to zero for which the condition $\tau_i \approx -\Delta T$ holds.

Furthermore, in case all phase detectors are sorted in an ascending order, i.e., $\tau_i \leq \tau_{i+1}$, the counter values v_i assume a V-shaped curve. Thus, X-ORCA might also be utilizing all phase detectors for reconstructing Δx by, for example, calculating the best-fitting-curve.

C. Real-World Implementation Details

The description presented in Subsection II-B has made a few, practically unrealistic assumptions, which are more or less concerned with the maximal frequency f that can be processed by the phase detectors. First of all, the X-ORCA concept has assumed that the clock frequency $\mathrm{clk} \geq 100 \times f$ is at least 100 times higher than the frequency of the localization signal $s(t)$ in order to achieve a practically relevant resolution. A signal frequency of $f = 100\,\mathrm{MHz}$, for example, would require a clock frequency of at least $\mathrm{clk} = 10\,\mathrm{GHz}$. Such a clock frequency, however, would be way too unrealistic for low-cost devices, such as FPGAs.

In case of periodic localization signals, however, a virtually very high frequency can be achieved by a technique, known as unfolding-in-time [6]. Let us assume, for example, a signal with frequency f and thus a period of $T = 1/f$. Then, the samples could be taken at $0, t, 2t, \ldots, (n-1)t$, with $t = T/n$ denoting the interval between two consecutive samples, and n denoting the number of samples per signal period T. Then, unfolding-in-time means that the samples are taken at $0, (t+T), 2(t+T), \ldots, (n-1)(t+T)$. That is, the sampling process is expanded over an extended interval with duration nT. Moreover, unfolding-in-time does not necessarily stick to

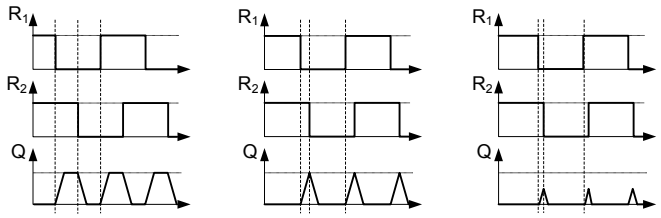

Fig. 5. Due to the inherent rise and fall times, a change in a gate's output requires some time. Therefore, if the input frequency increases too much or if the input edges come too close together, the gate cannot properly change its output (right-hand-side).

an increment of "$t + T$". For example, the samples can also be taken at $0, (kt+T), 2(kt+T), \ldots, (n-1)(kt+T)$, with k denoting a constant that is prime to n.

The second assumption concerns the electrical transition behavior of the XOR gates as well as the counters. The conceptual description of Subsection II-B implicitly assumes that gates and counters are fast enough to properly process signals that travel along the internal wires with about two third of the speed of light. The technical suitability of this approach might be surprising to some readers but has already been shown in previous research [2]: due to technical reasons, such as thermal noise, the logic gates do not yield exact results but a rather randomized behavior if, for example, set and hold time requirements are not met. This random effect can be *statistically* compensated, for example, by a large number of processing elements. This is another reason for the X-ORCA architecture to employ a rather *large* number of phase detectors.

The third implementation remark concerns the processing speed of the gates and the input parts of the counters. Figure 5 shows that if the phase shift gets too small (or too close to $180°$), the rise and fall times prevent the gate from properly switching its output state. This effects lead to small errors of the counter values, if the phase shift $\Delta\varphi$ is close to zero or $180°$; as a result, the expected V-shaped curve of the counter values (subsection II-B) might change to a U-shape.

III. Methods

The first X-ORCA prototype was implemented on an Altera Cyclone II FPGA [5]. This device offers 33,216 logic elements and can only be clocked at about 85 MHz. The chosen FPGA *development board* is a low-cost device that charges about 500 USD.

Figure 6 shows a top-level view of the X-ORCA prototype. It consists of 140 phase detectors, a common data bus, a Nios II soft core processor [7], and a system PLL that runs at 85 MHz. The Nios II processor manages all the counters of the phase detectors, and reports the results via an interface to a PC (not shown). The internal "delay wires" w_1 and w_2 are realized as pure passive internal wires, connecting the device's logic elements, as previously announced in Subsection II-B.

The practical experiments can be classified into two groups. In the first group, the localization signal $s(t)$ was generated

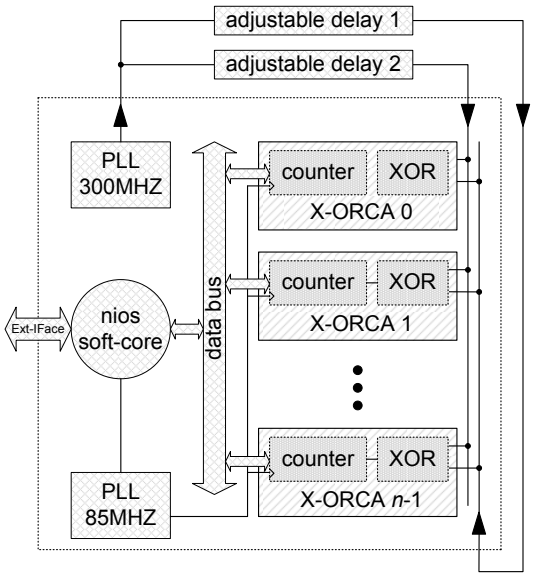

Fig. 6. On the top-level, the X-ORCA implementation consists of 140 phase detectors (aligned from top to bottom), a Nios II processor, a first PLL for the system, a second PLL for the localization signal with a frequency of 300 MHz, and just a little bit of additional infrastructure.

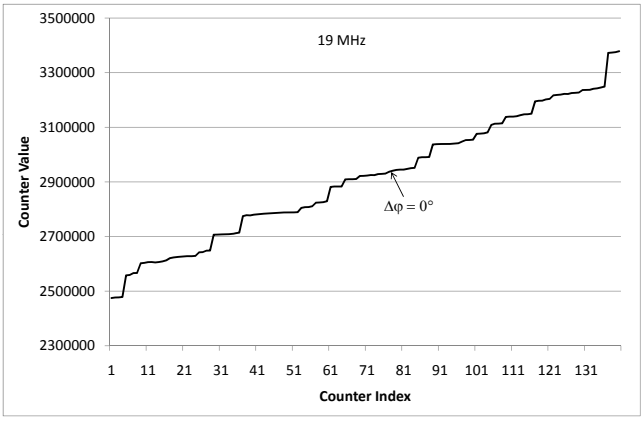

Fig. 7. This figure shows the counter values v_i of $n = 140$ phase detectors when exposed to two 19 MHz signals with zero phase shift $\Delta\varphi = 0$.

by an external signal generator which was connected to the system by means of a power splitter, a regular cable, and a line stretcher [8]. In this setup, the available laboratory equipment allows for frequencies of up to 19 MHz only. The second group consists of signals with up to 300 MHz. In these experiments, the localization signal $s(t)$ was realized by means of a second PLL, which runs at 300 MHz (upper-left corner of Fig. 6), and the distances were emulated by active delay lines, which restrict the length differences Δx to a small set of discrete values.

It should be noted that no wireless communication module was used in order to focus on the properties of the actual X-ORCA hardware system.

IV. Results

The prototype was tested in series of practical experiments which had three aims: (1) validation of the X-ORCA concept, (2) exploring the upper limits of the localization signal's frequency f with which the prototype is still working properly, and (3) finding the lower limit of the normalized time shift $\Delta t/f$ for which the prototype yields reasonable results. All the results of these experiments are summarized in Figs. 7-13. All the figueres show $n = 140$ different phase detectors, which were clocked at a rate of 85 MHz.

Concept validation: In the first validation experiment, the prototype was receiving two 19 MHz localization signals that had a zero phase shift $\Delta\varphi = 0$ and that were emitted by an external function generator. Figure 7 shows the values of the $n = 140$ counters after 1,000,000 samples taken with the 85 MHz system clock. In this configuration, taking 1,000,000 samples corresponds to an averaging over 619 periods with virtually 1615 samples per period of the localization signal (please, see also the discussion presented in Subsection II-C). It can be seen that the counters assume quite monotonically increasing values v_i.

In addition to the pure validation of the concept, Fig. 7 reveals some technological FPGA internals that might be already known to the expert readers: neighboring logic elements do not necessarily have equivalent technical characteristics and are not interconnected by a regular wire grid. As a consequence, the counter values v_i and v_{i+1} of two neighboring phase detectors do not steadily increase or decrease, which makes the curve look a little rough.

Furthermore, the prototype's internal delays τ_i do not span the times of an entire period of the 19 MHz signal. Consequently, Fig. 7 shows only a small part of a complete V-shape. In addition, by considering the counter values in relation to the total number of samples taken, the calculation of the minimal and maximal internal time delays easily arrive at $\tau_{\min} = 6.5$ ns $\tau_{\max} = 8.9$ ns, respectively.

Figure 8 presents the same results of of Fig. 7 but enhanced with two additional external phase shifts $\Delta\varphi \approx -0.3°$ (dashed line), and $\Delta\varphi \approx +0.3°$ (dotted line). It can be clearly seen that a time shift of $\Delta t = (0.3°/360°)/(19\,MHz) = 0.044$ ns changes all counters by approximately 40,000.

Upper limit of the signal frequency f: The available laboratory equipment did not allow for localization frequencies f larger than 19 MHz. Therefore, the second set of experiments utilized a second system-internal PLL (see, also, Fig. 6), which runs at 300 MHz.

Figure 9 shows the $n = 140$ counter values v_i for two 300 MHz (localization) signals that have a zero phase shift $\Delta\varphi = 0$ (solid line), a phase shift $\Delta\varphi = -43°$ (dotted line), and a phase shift $\Delta\varphi = +43°$ (dashed line). The input signals were sampled 1,000,000 times, which corresponds to an averaging over 196 periods, with virtually 5100 samples per period of the localization signal (please, see also the discussion presented in Subsection II-C). It can be clearly seen that the minimum is at counter #31 with increasing counter values to the right and left as can be expected from X-ORCA's internal

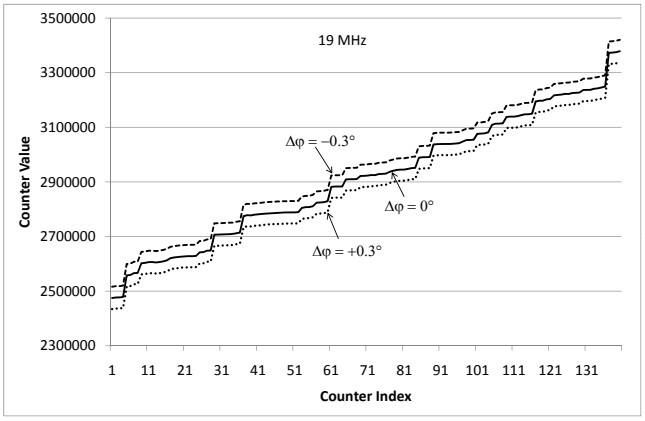

Fig. 8. This figure shows the counter values v_i of $n = 140$ phase detectors when exposed to two 19 MHz signals with zero phase shift $\Delta\varphi = 0$ (solid line), with phase shift $\Delta\varphi \approx -0.3°$ (dashed line), as well as with phase $\Delta\varphi \approx +0.3°$ (dotted line).

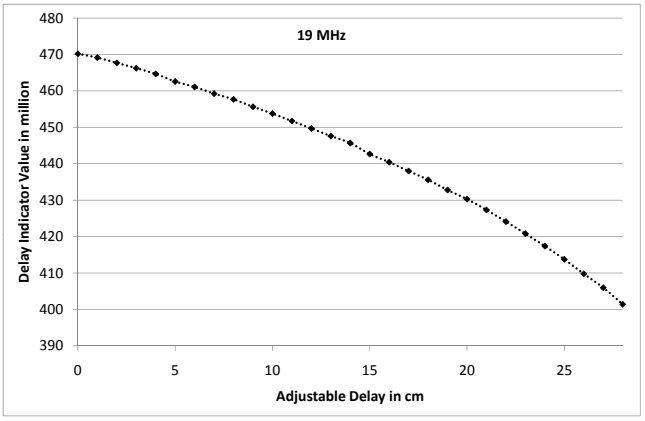

Fig. 10. The figure shows the delay value indicator when employing two 19 MHz localization signals. The data points results from varying length of the employed line stretcher.

architecture.

Figure 9 shows the same qualitative behavior already shown in Fig. 8. That is, already the first prototype is able to determine the phase shift of two 300 MHz signals, even though these signals are sampled at only 85 MHz. The figure also shows that a time difference of $\Delta t = 0.4\,\mathrm{ns}$ consistently shifts the "counter curve" by about 20 counters. This results *suggests* that at 300 MHz, the prototype would be able to detect a time delay as small as $\Delta t = 0.02\,\mathrm{ns}$, which equals to a length resolution of about $\Delta x \approx 5\,\mathrm{mm}$.

Unfortunately, the available FPGA device does not allow for higher frequencies of the localization signal, and thus does not allow for finding the true limits for f. Furthermore, a closer look at Fig. 9 reveals that the graphs are not exactly V-shaped but rather U-shaped at their very bottom. This is because the effects already discussed in Fig. 5 come into effect.

Lower limit of $\Delta t/f$: The third focus of the practical experiments was to explore the lower limit of the normalized time delay $\Delta t/f$. To this end, the prototype was exposed to two localization signals with varying time delays. The localization frequencies were set to $f \in \{19\,\mathrm{MHz}, 1.14\,\mathrm{MHz}, 111\,\mathrm{kHz}, 11\,\mathrm{kHz}\}$. The results are plotted in Figs. 10-13. In order to make the figures readable, they all present the *delay value indicator*. This indicator is simply the sum of all the $n = 140$ counter values v_i. In other words, a single graph in the previous performance figures is collapsed into one single point. In all the experiments, the line stretcher was 29 times extended by 1 cm.

All the four figures show the very same qualitative behavior. The only difference is the absolute value of the delay value indicator: a decrease of the localization frequency by a factor of 10 leads to a reduction of the delay value indicator by the very same value, since with the identical time delay Δt the phase shift is only a tenth, if the frequency is also just a tenth.

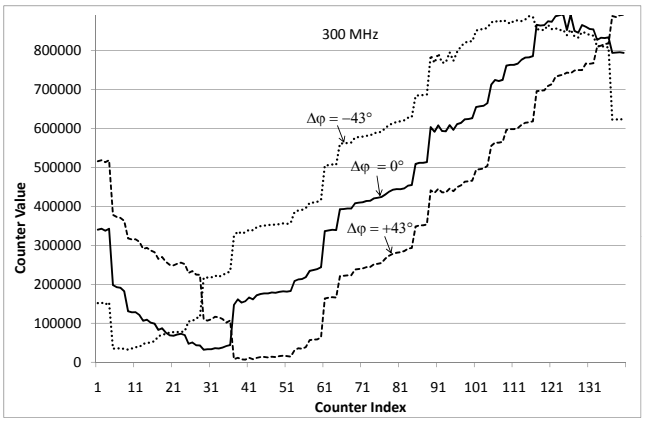

Fig. 9. The figure shows the counter values v_i of $n = 140$ phase detectors when fed with two 300 MHz signals with zero phase shift $\Delta\varphi = 0$ (solid line), with a phase shift $\Delta\varphi = -43°$ (dotted line), as well as with a phase shift $\Delta\varphi = +43°$ (dashed line).

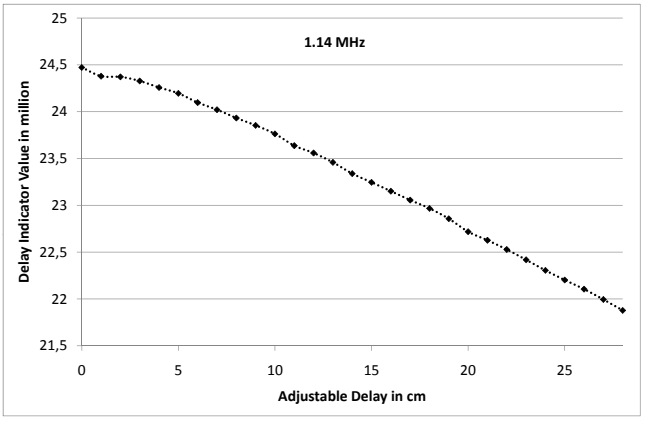

Fig. 11. The figure shows the delay value indicator when employing two 1.14 MHz localization signals. The data points results from varying length of the employed line stretcher.

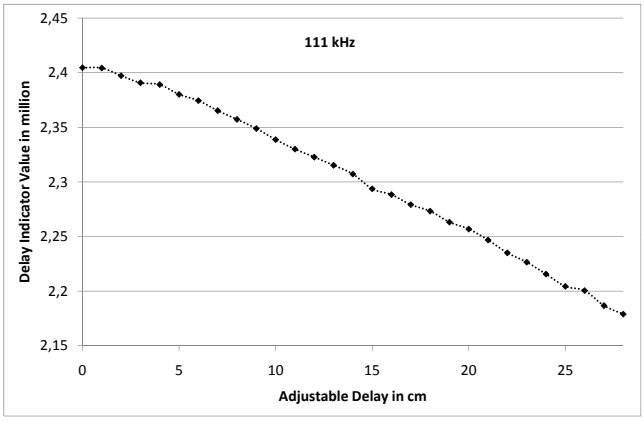

Fig. 12. The figure shows the delay value indicator when employing two 111 kHz localization signals. The data points results from varying length of the employed line stretcher.

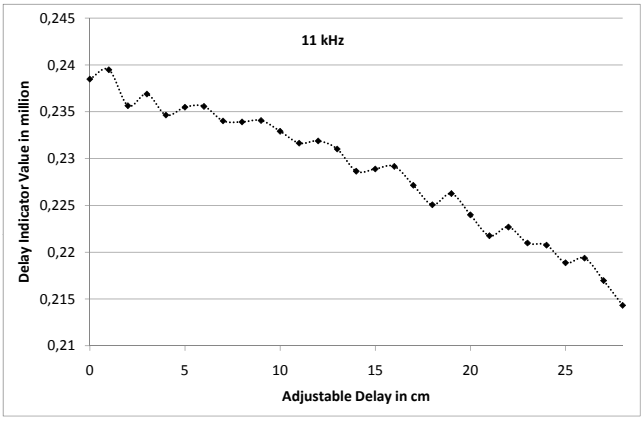

Fig. 13. The figure shows the delay value indicator when employing two 11 kHz localization signals. The data points results from varying length of the employed line stretcher.

V. Discussion

This paper has presented a new localization architecture, called X-ORCA. X-ORCA that is highly inspired by the barn owl auditory system. Its main purpose is the localization of transmitters, such as WLAN network cards or Bluetooth dongels, that emit electromagnetic signals. In its core, X-ORCA consists of a large number of very simple phase detectors, which are mounted along two passive wires with very small but finite internal time delays. This large number of rather unreliable phase detectors allows X-ORCA to perform a rather *reliable* statistical evaluation.

The first prototype was implemented on an Altera Cyclone II FPGA. It has already shown that X-ORCA can easily determine the phase shift of two 300 MHz signals; in light of the 85 MHz clock frequency, the result might be a bit surprising to some readers. It merely indicates that (1) the counters can be *virtually* clocked at the desired high frequency and that (2) the internal passive wires indeed lead to effective time delays τ_i that can be evaluated by the very same device in a *digital* form.

Unfortunately, the available laboratory equipment did not allow for testing the true limits of the first prototype. This particularly applies to the maximal frequency f of the localization signal and to the achievable resolution with respect to Δx. These tests will be subject of future research.

This paper deliberately does not present any comparison with existing (indoor) localization systems, such as Ubisense [9], GPS [10], and iLoc [11], since the overall localization accuracy also depends on variaous other factors, such as the radio transmitters and receicers, the environment, the presence of obstacles, etc. Rather, this paper focuses only on the phase and time resolution on the pure technical level in order to avoid any unfair comparison.

Future research will also be devoted to the integration of wireless communication modules. The best option seems to be the utilization of a software-defined radio module, such as the Universal Software Radio Peripheral 2 (USRP2) [12]. Finally, future research will port the first prototype onto more state-of-the-art development boards, such as an Altera Stratix V FPGA [13].

Acknowledgements

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