MBMV06

9. Workshop Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen
Dresden, Germany

Reduction of Leakage Currents with Mixed Gates in Deep Submicron Technologies

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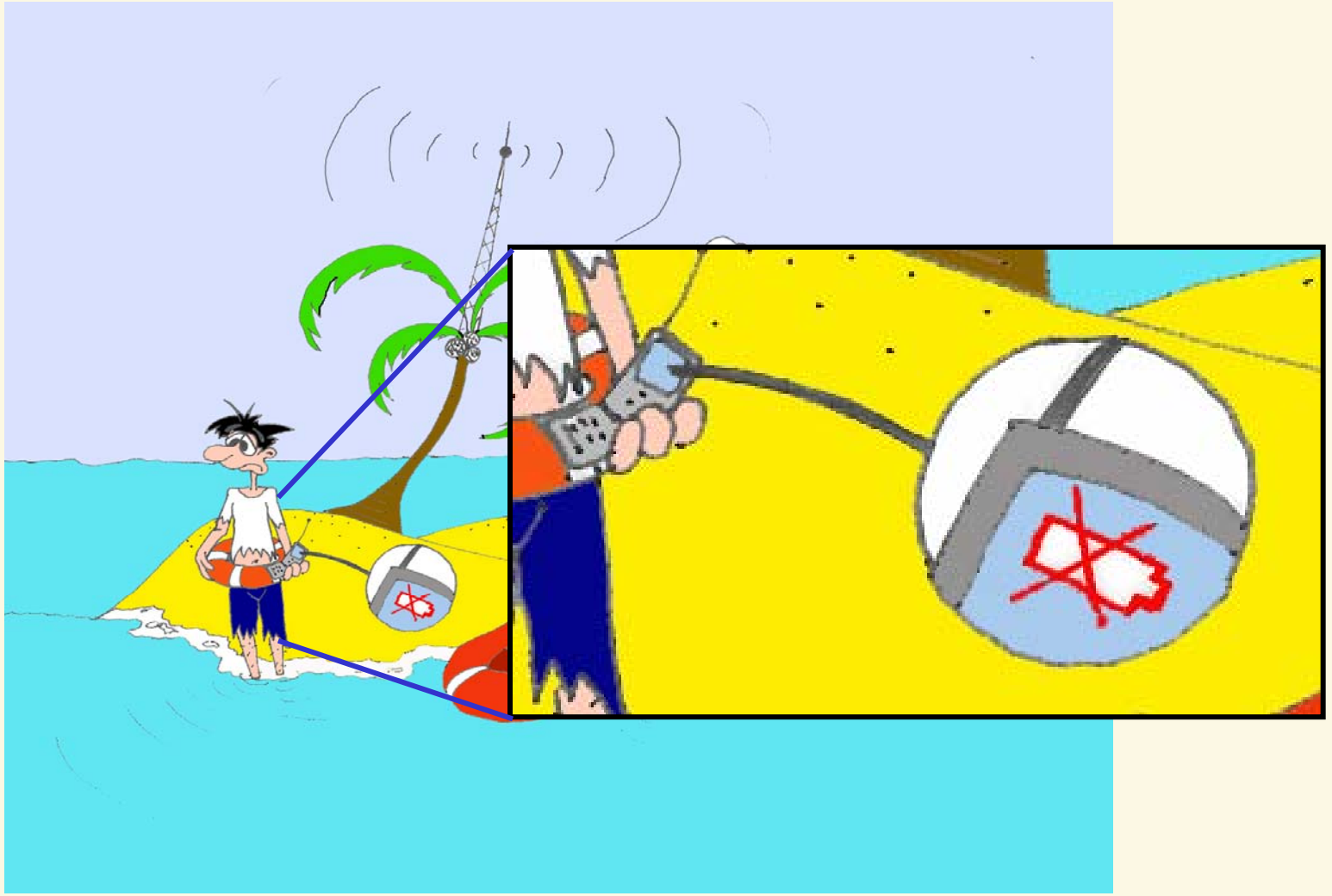
Outline

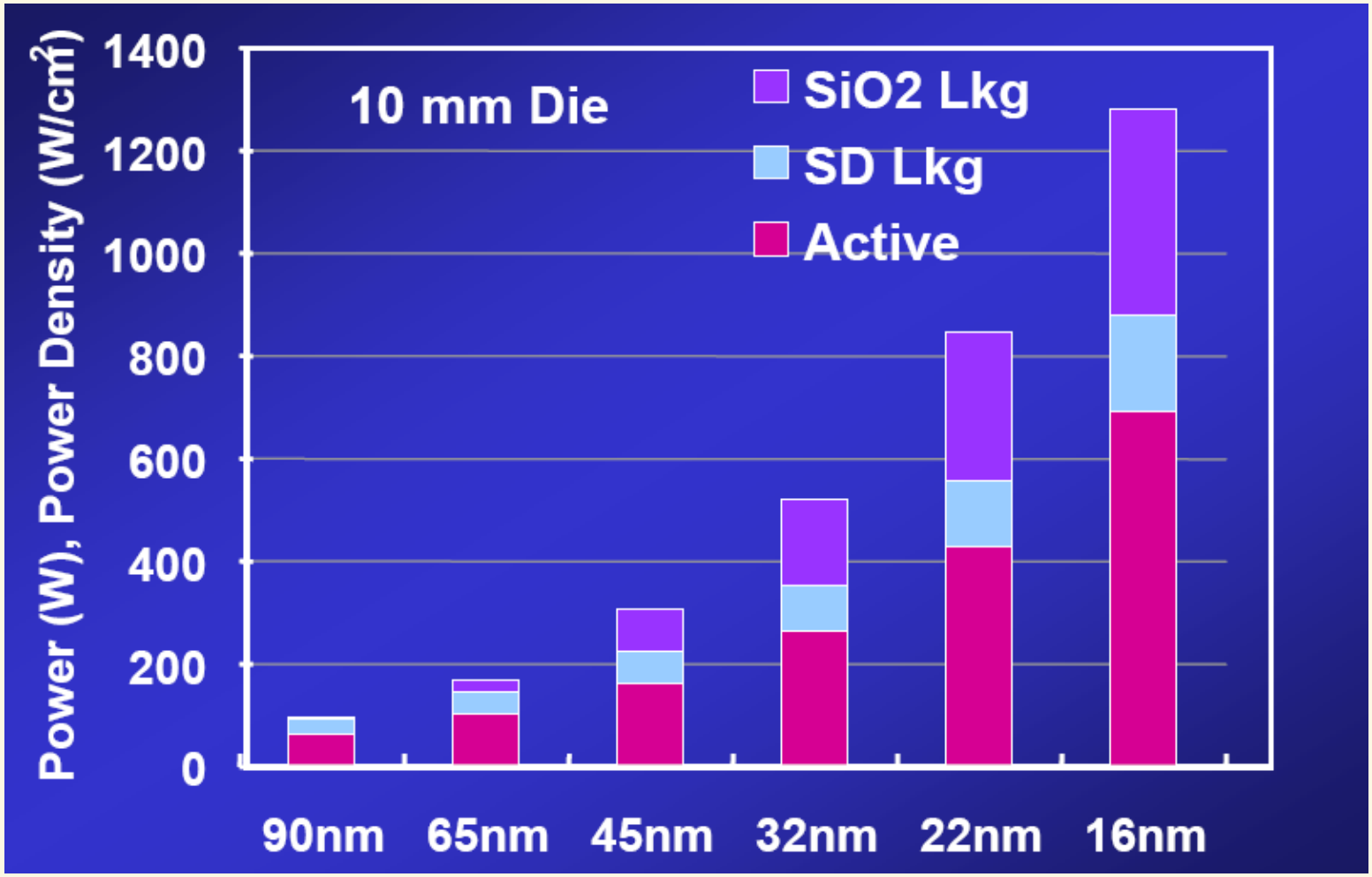
1. Motivation
2. Basics
3. Mixed Gates
4. Algorithm
5. ISCAS – Benchmarks
6. Conclusion

1. Motivation

Why Thinking about Leakage?



Trend: Power



S. Borkar, '05

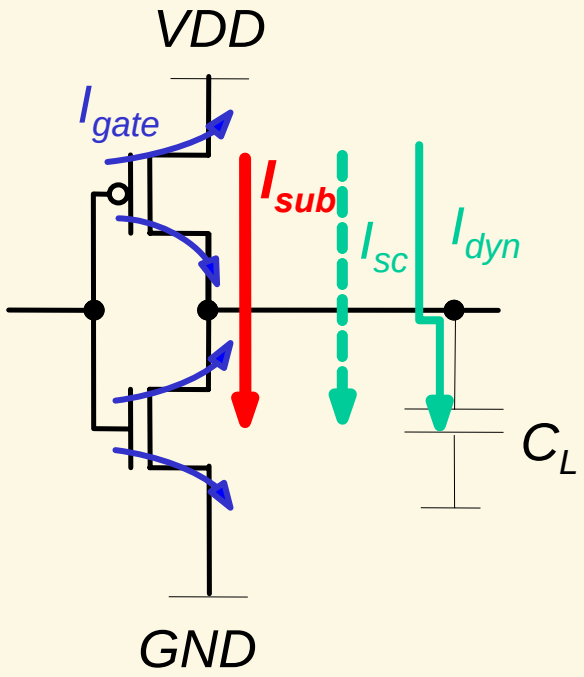
Focus of this Work

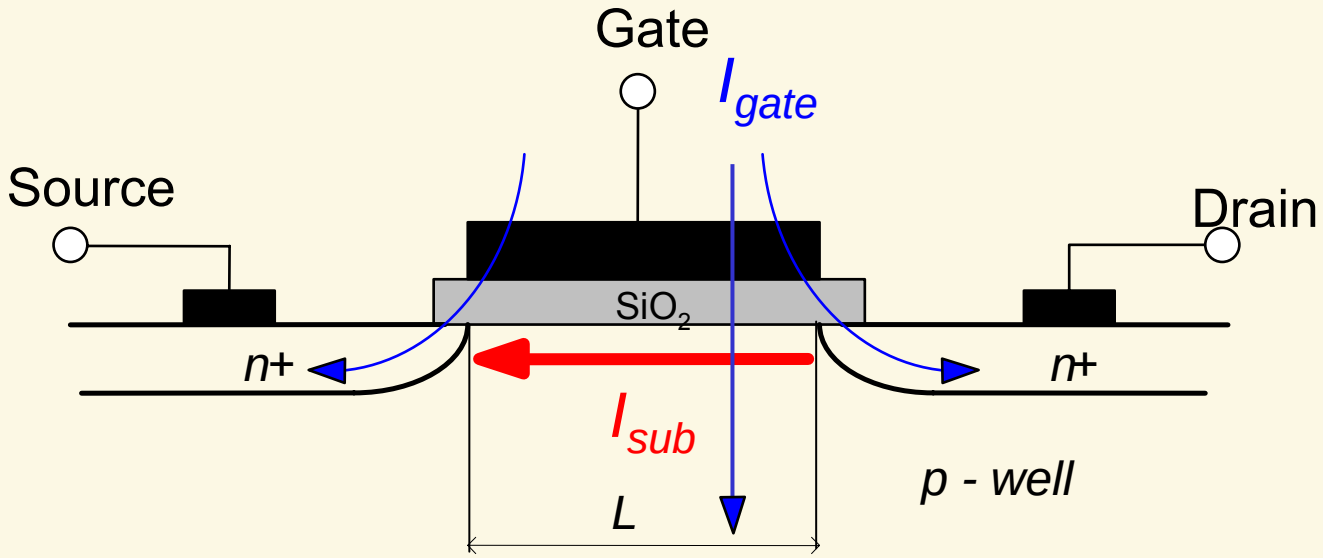
1. Modification of established Leakage Reduction Approach (DTCMOS)

2. Allocation algorithm

2. Basics

Power Dissipation in CMOS



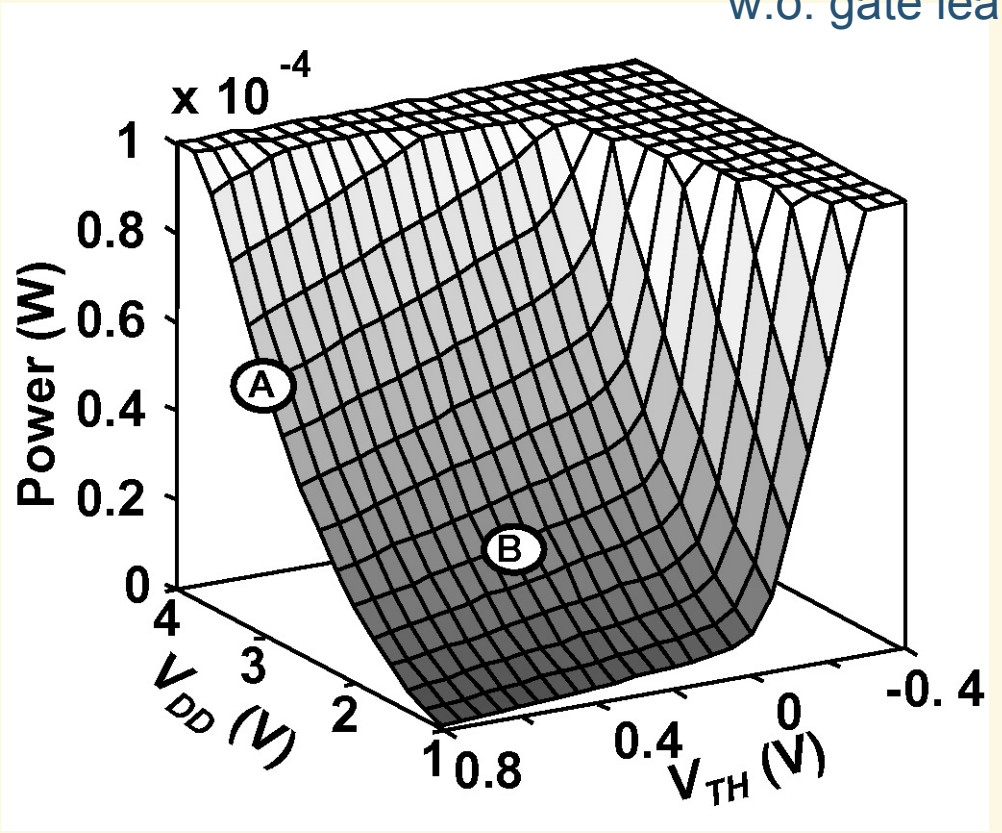


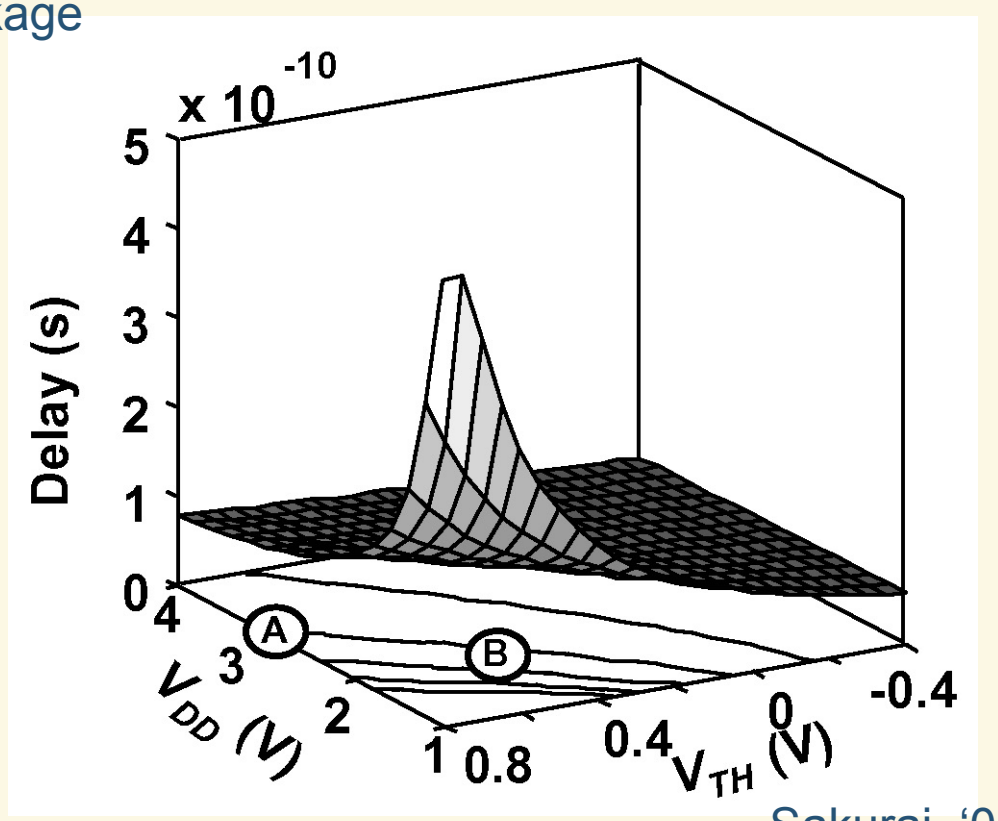
- I_{sub} occurs if $V_g < V_{th}$
- carriers move by diffusion along surface
- I_{gate} caused by direct tunneling through gate oxide

Power & Delay Dependence

$$P = p_t \cdot f_{CLK} \cdot C_L \cdot V_{DD}^{\,2} + I_0 \frac{W_T}{W_0} \cdot 10^{\frac{-V_{TH}}{S}} \cdot V_{DD} \qquad t_d = \frac{k \cdot Q}{I} = \frac{k' \cdot C_L \cdot V_{DD}}{(W/L) \cdot (V_{DD} - V_{TH})^{\alpha_K}}$$

w.o. gate leakage





Sakurai, '01

Power & Delay Dependence

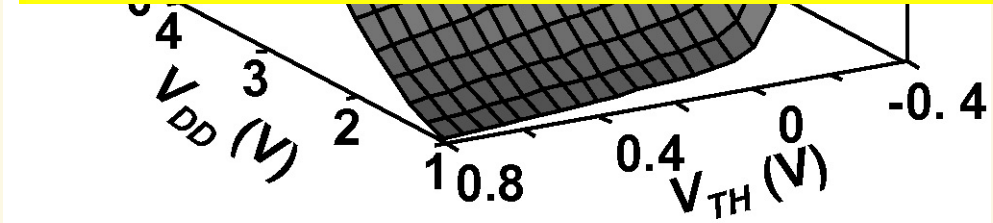
$$P = p_t \cdot f_{CLK} \cdot C_L \cdot V_{DD}^{\,2} + I_0 \frac{W_T}{W} \cdot 10^{\frac{-V_{TH}}{S}} \cdot V_{DD} \qquad t_d = \frac{k \cdot Q}{I} = \frac{k' \cdot C_L \cdot V_{DD}}{(W/L) \cdot (V_{DD} - V_{TH})^{\alpha_K}}$$

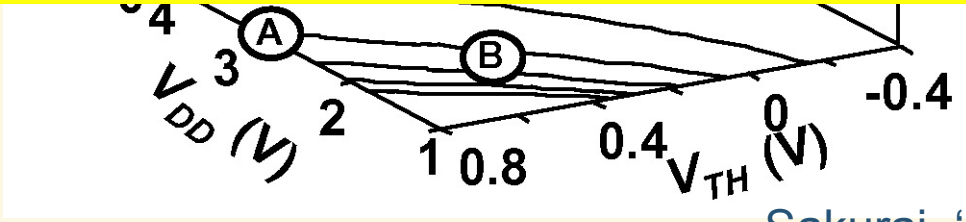
Problem:

fast transistors with high power dissipation (low V_{th})

or

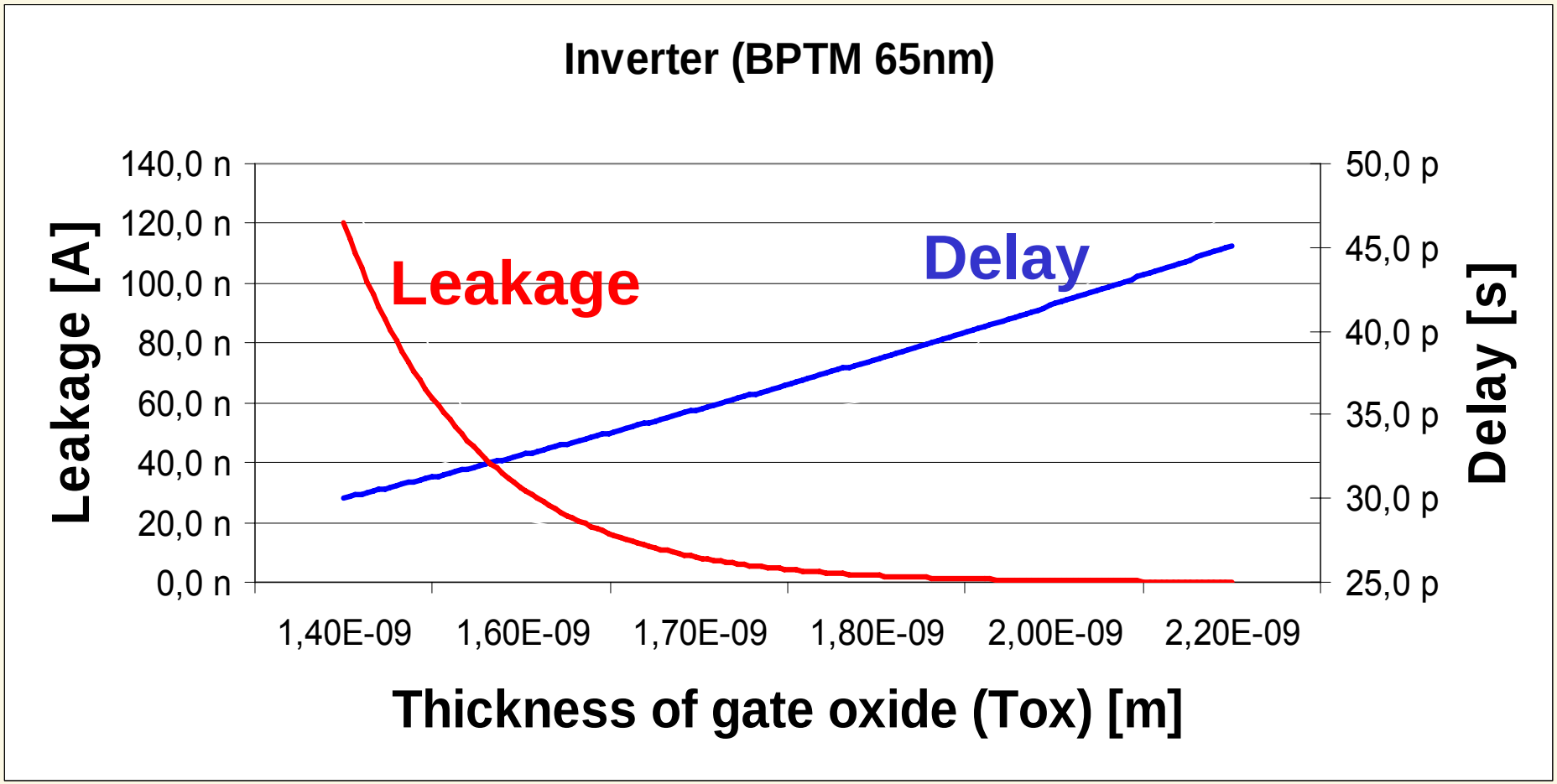
slow transistors with low power dissipation (high V_{th})



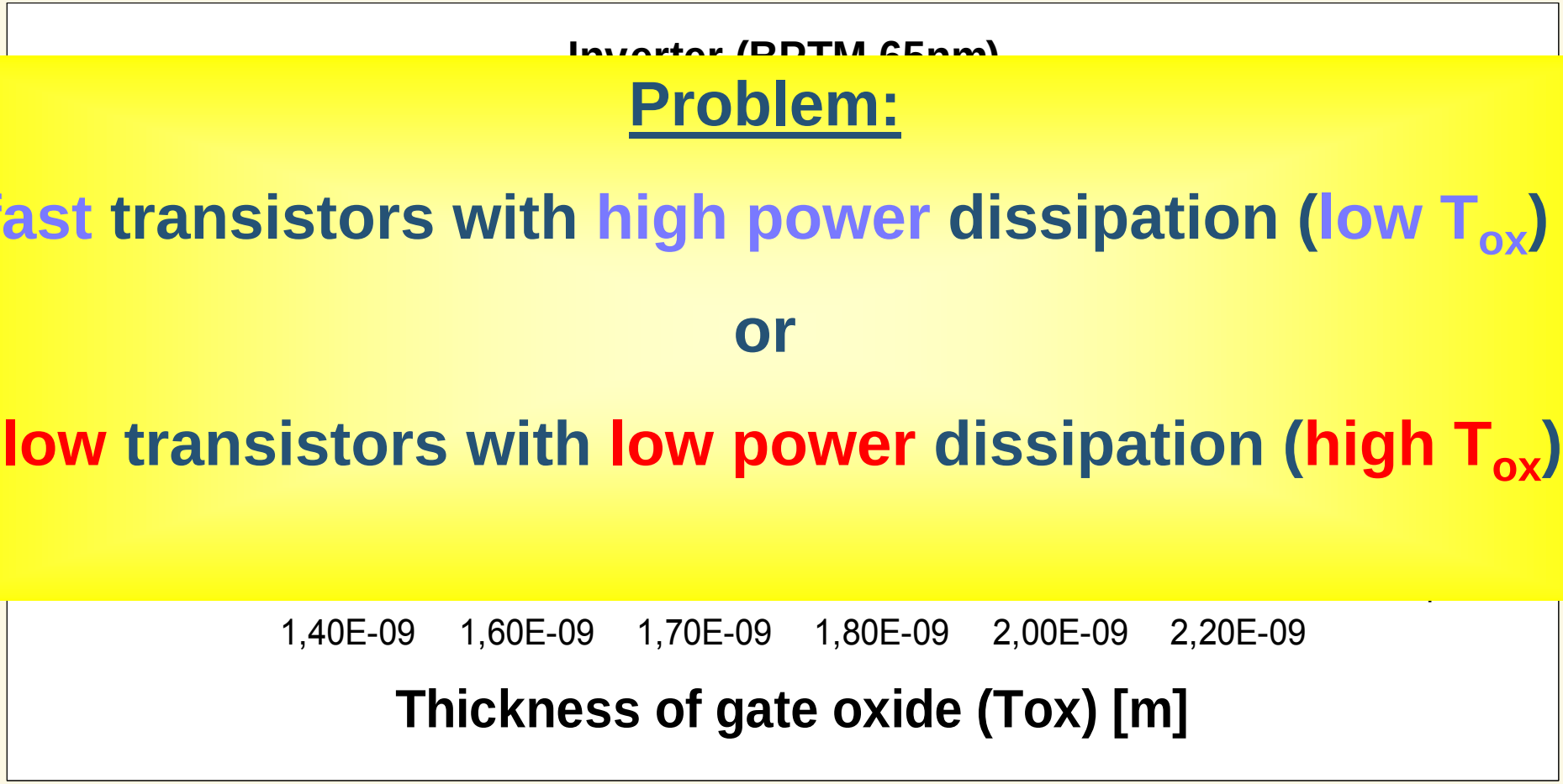


Sakurai, ‘01

T_{ox} vs. Delay and Leakage



T_{ox} vs. Delay and Leakage



Problem:

fast transistors with high power dissipation (low T_{ox})

or

slow transistors with low power dissipation (high T_{ox})

Dual V_{th} (DTCMOS) / Dual T_{ox} (DToCMOS)

- Use different V_{th}'s / T_{ox}'s
  - use lower V_{th} / T_{ox} for devices on the critical paths
  - use higher V_{th} / T_{ox} for devices off the critical paths
- Decrease power without performance penalty
- Approaches at:
  - Gate level (V.Sundararajan et al., LPED'99)
  - Transistor level (L.Wei et al., DAC'99)

3. Mixed Gates

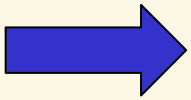
Mixed Pull-*Down/Up*-Paths

Goal (for fast gates): keep the delay while leakage decreases

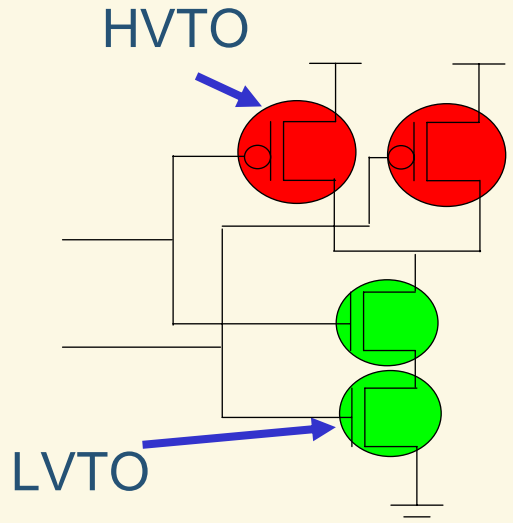
if all transistors in gates are dimensioned regularly
(= PMOS and NMOS have same resistance)

⟶ different output slopes

up to now: sizing of transistors



idea: use different V_{th} / T_{ox} within a gate to adapt the slopes



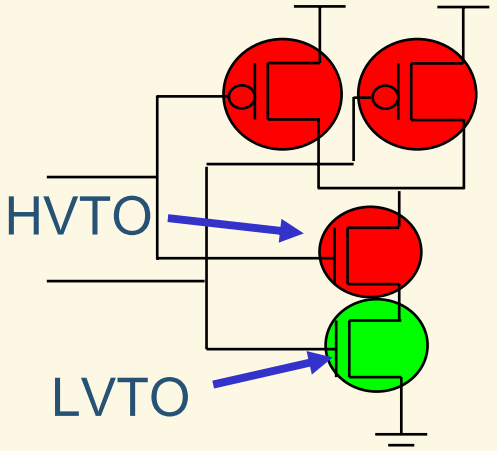
Mixed Stacks

Goal: additional gate types at constant mask count

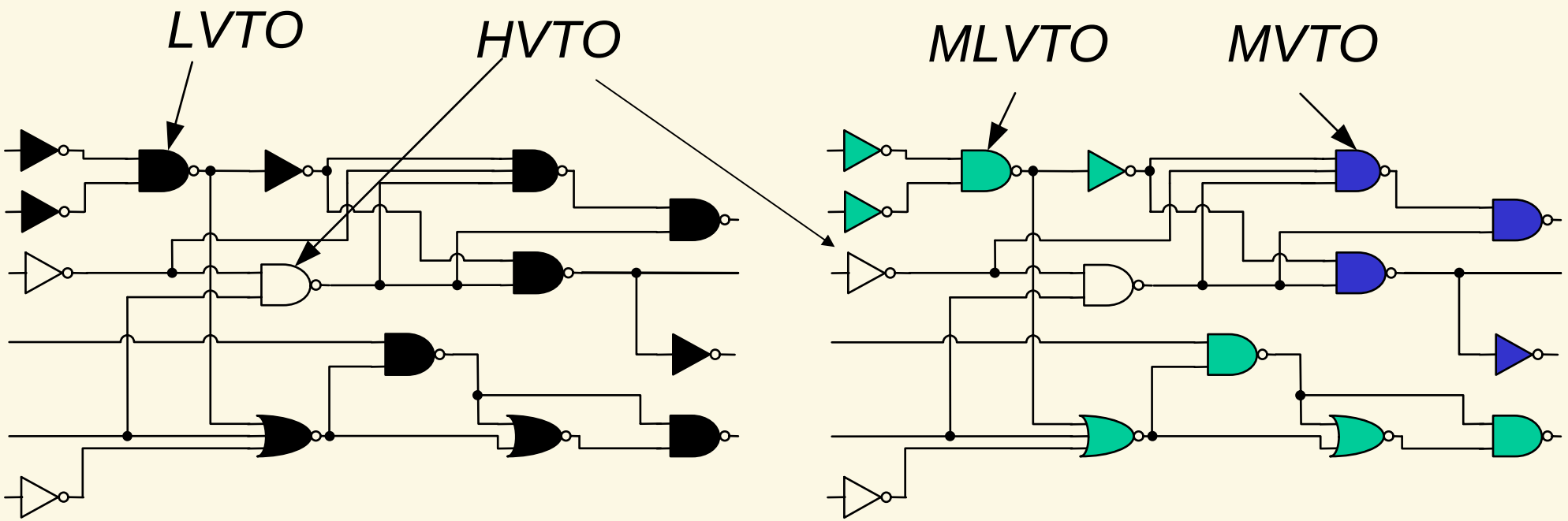
only two gate types in DTCMOS / DToCMOS at gate level (HVTO, LVTO)

→ problem: more LVTO gates after optimization as needed to keep the delay

idea: mixed V_{th} / T_{ox} within a gate (stack & Pull-up/Pull-down path)



MG - Paths

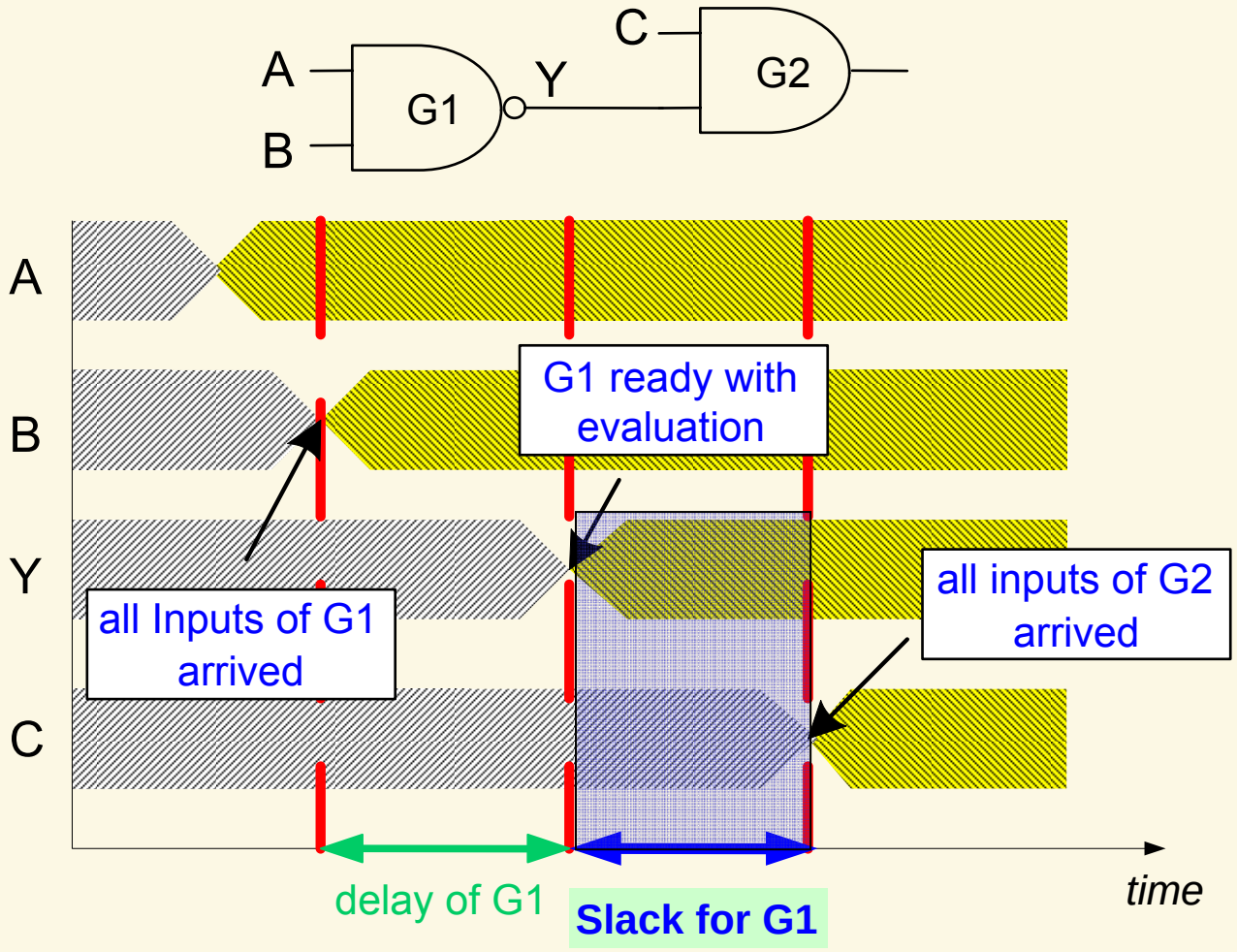


Up to now: *two kinds of cells*
(DTCMOS/DToCMOS)

MG-CMOS

4. Algorithm

Slack


A
B
G1
Y
C
G2
A
B
Y
C
G1 ready with evaluation
all Inputs of G1 arrived
all inputs of G2 arrived
delay of G1
Slack for G1
time

Weight ψ_n

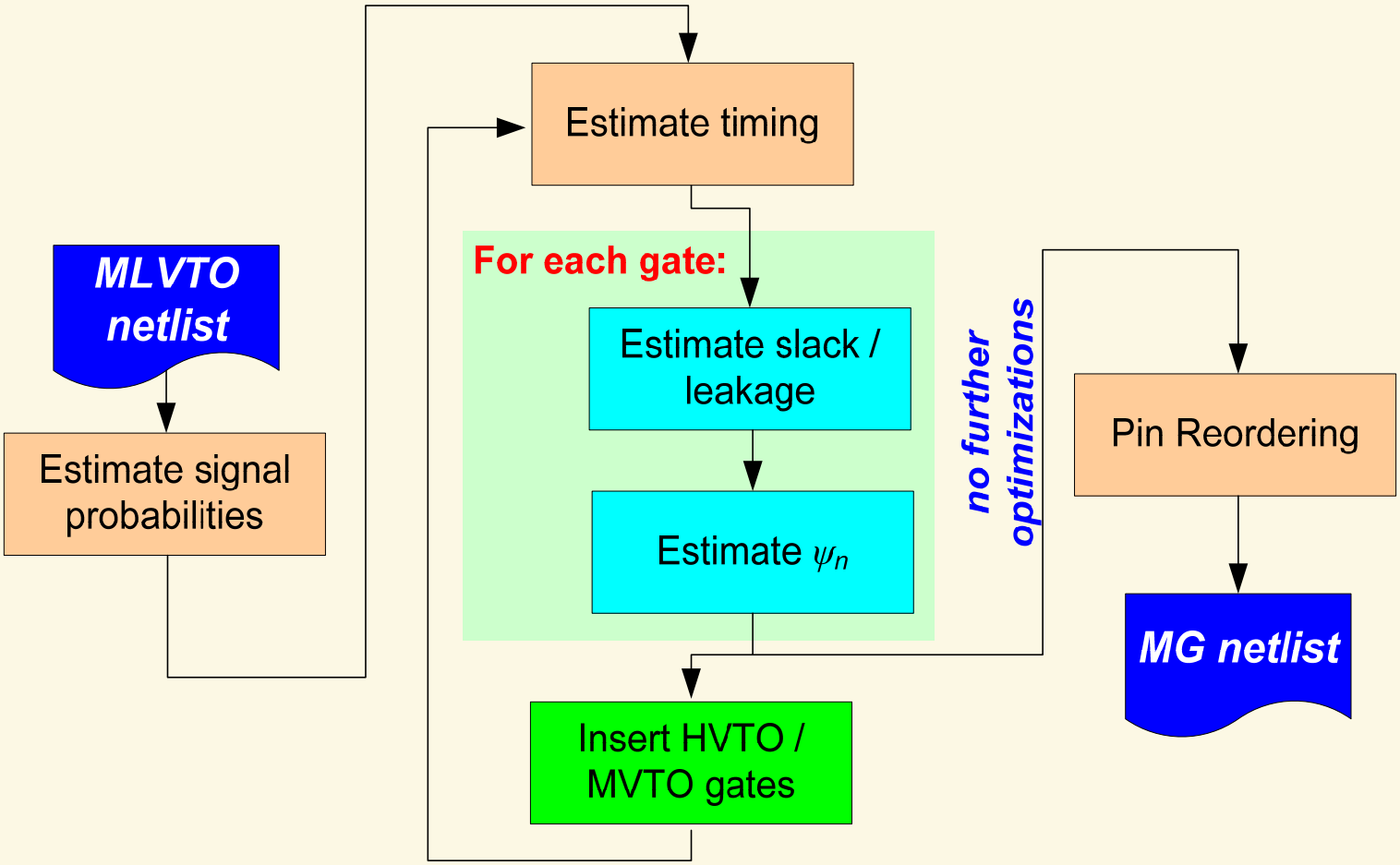
$$\psi_n = I_{leak\_diff} \cdot \left(1 + t_{slack} - t_{diff}\right) \cdot \left(pos_{weight}\right)^{-0.5}$$

I_{leak_diff} = difference of leakage of weighted gate type compared to leakage of current gate type

t_{diff} = difference of delay of weighted gate type compared to delay current gate type

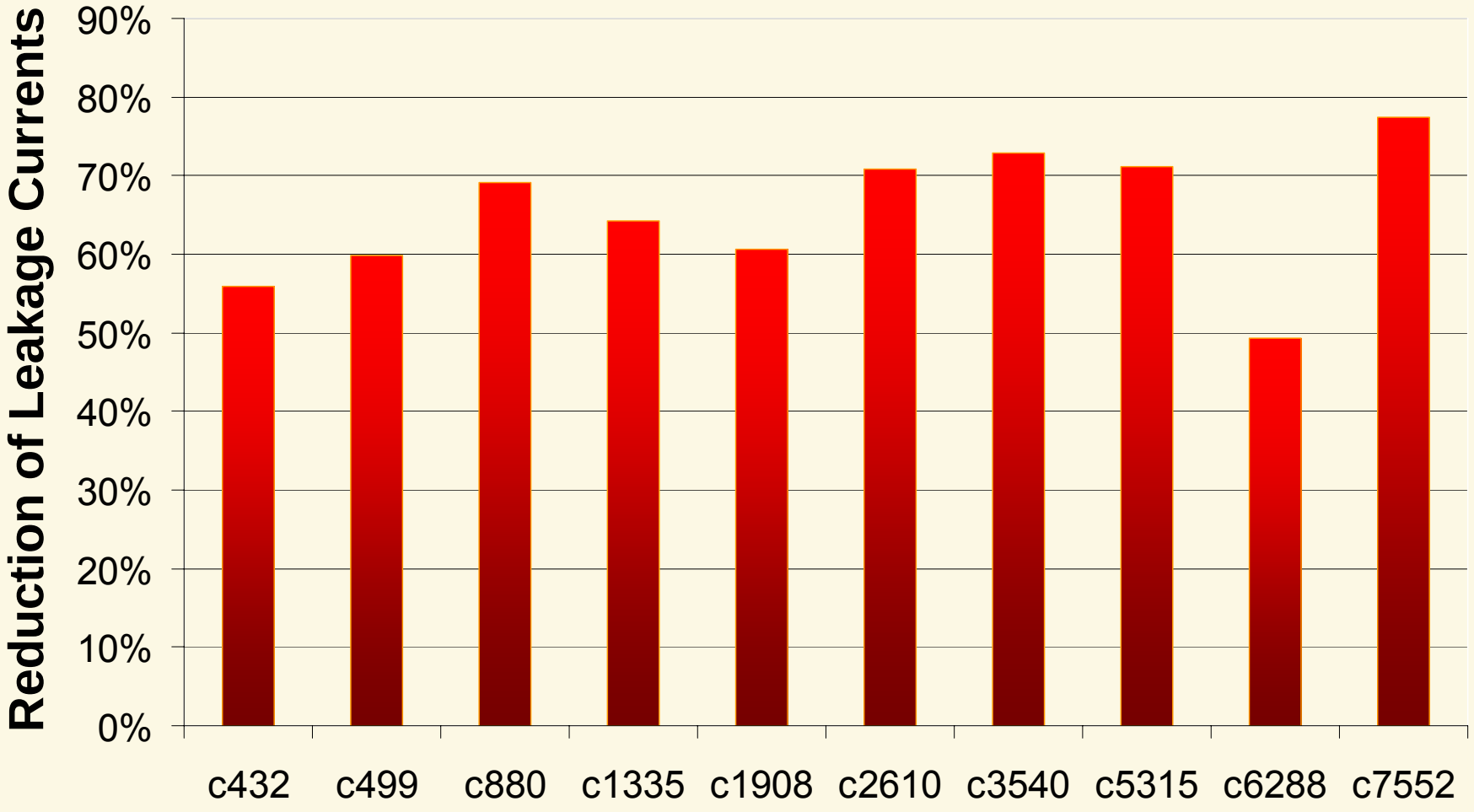
$pos_{weight} = \Sigma_{gate\_inputs} + \Sigma_{connected\_gates\_on\_output}$

Allocation algorithm

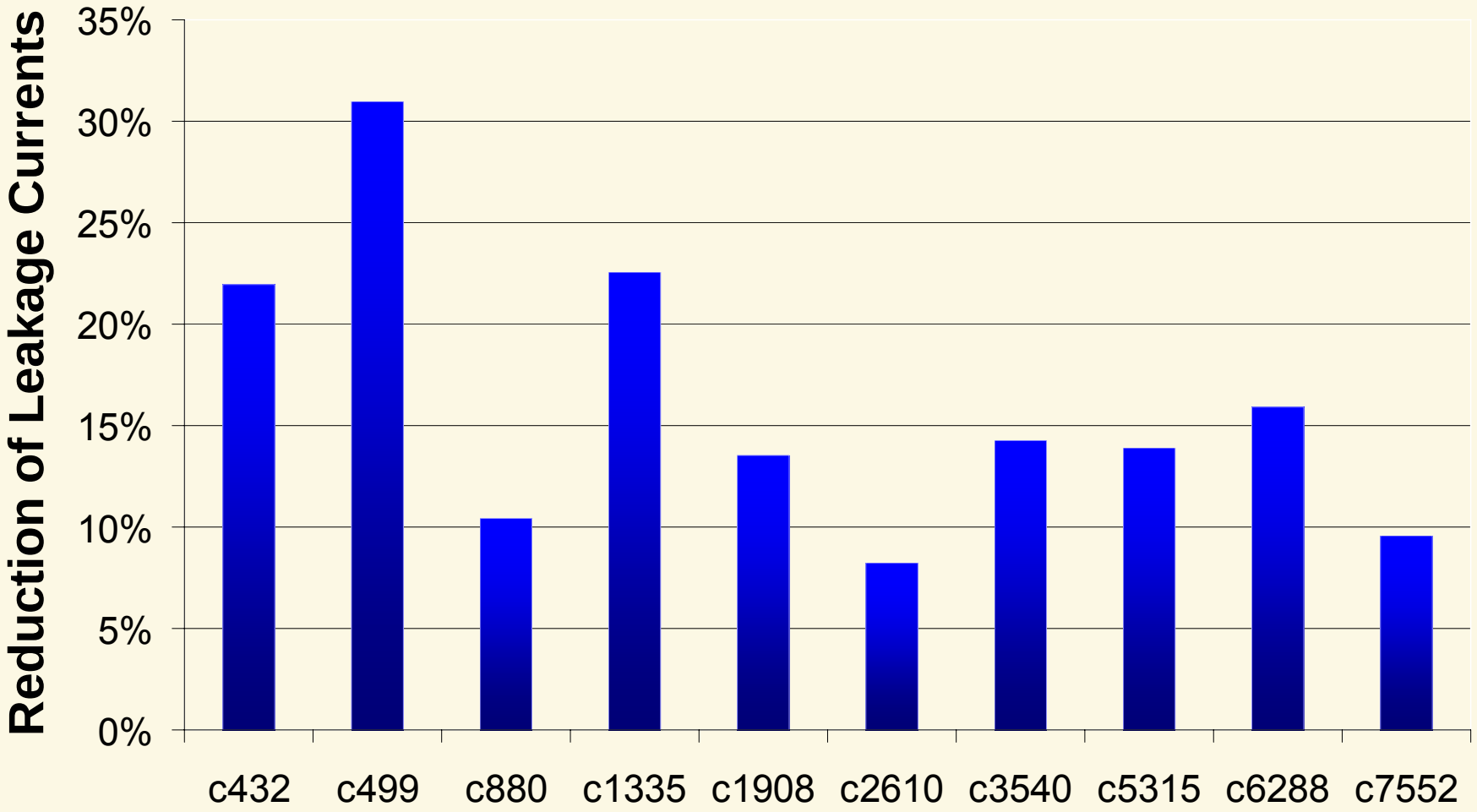


5. ISCAS - Benchmarks

LVT vs. MG


Reduction of Leakage Currents
90%
80%
70%
60%
50%
40%
30%
20%
10%
0%
c432
c499
c880
c1335
c1908
c2610
c3540
c5315
c6288
c7552

DTCMOS vs. MG


Reduction of Leakage Currents
35%
30%
25%
20%
15%
10%
5%
0%
c432
c499
c880
c1335
c1908
c2610
c3540
c5315
c6288
c7552

5. Conclusion

- Subthreshold current and gate oxide leakage dominate leakage power
- Mixed Gates (MG) combine advantages of DTCMOS and DToCMOS at transistor and gate level
- Average 65% *(vs. LVT)* and 18% *(vs. DTCMOS)* leakage reduction at constant delay

Thank you!

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