Low Power Gate-level Design with Mixed-$V_{th}$ (MVT) Techniques

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Outline

1) Motivation
2) Basics
3) Different Threshold Voltages
4) Application of Mixed-$V_{th}$
5) Conclusion
1. Motivation
Trend: Performance

MIPS


8080

8086

386

Pentium® proc

Pentium® 4 proc

1 TIPS

Intel, ‘03
Trend: Power

Intel, '03
Dynamic Power vs. Leakage

![Graph showing dynamic and static power dissipation across different technologies and voltages.]

Intel, '02
2. Basics
Power Dissipation in CMOS

- $I_{sub}$ occurs if $V_g < V_{th}$
- carriers move by diffusion along the surface
- $I_{sub}$ dominates leakage
**Power & Delay Dependence**

\[ P = p_t \cdot f_{CLK} \cdot C_L \cdot V_{DD}^2 + I_0 \cdot \frac{W_T}{W} \cdot 10^{-\frac{V_{TH}}{S}} \cdot V_{DD} \]

\[ t_d = \frac{k \cdot Q}{I} = \frac{k' \cdot C_L \cdot V_{DD}}{(W / I) \cdot (V - V_{TH})^{\alpha_k}} \]

**Problem:**

- fast transistors with high power dissipation (low \( V_{th} \))
- slow transistors with low power dissipation (high \( V_{th} \))

Sakurai, ‘01
3. Different Threshold Voltages
Dual Threshold Voltages (DTCMOS)

- Use different $V_{th}$’s
  - use lower threshold for devices on the critical paths
  - use higher threshold for devices off the critical paths
- Decrease power without reduce performance
- Approaches at:
  - Gate level (V. Sundararajan, et al., LPED’99)
  - Transistor level (L. Wei, et al., DAC’99)
DTCMOS on Different Levels

Transistor level
+ optimization is accurate
- needs a lot of resources
- not useful for considerably designs

Gate level
+ less time-consuming
- fewer detailed, because only two gate types
New Approach: Mixed-$V_{th}$ (MVT) CMOS

1. **Goal:** fast gates keep the delay while leakage decreases

- if all transistors in gates are standard dimensioned
  ( = PMOS and NMOS have same delay)
→ different output slopes
- up to now: sizing of transistors

**idea:** use different threshold voltages within a gate to adapt the slopes
2. **Goal:** additionally gate types at constant mask count

- only two gate types in DTCMOS at gate level (HVT, LVT)
- problem: more LVT gates after optimization as needed to keep the delay

*idea:* mixed threshold voltages within a gate
**MVT- NAND2**

<table>
<thead>
<tr>
<th>LVT gate</th>
<th>M-LVT gate</th>
<th>MVT gate</th>
<th>HVT gate</th>
</tr>
</thead>
<tbody>
<tr>
<td>- all MOS have low $V_{th}$</td>
<td>- PMOS have high $V_{th}$</td>
<td>- PMOS and upper NMOS have high $V_{th}$</td>
<td>- all MOS have high $V_{th}$</td>
</tr>
<tr>
<td>- rise time is shorter than fall time</td>
<td>- rise and fall time are nearly the same</td>
<td>- middle delay cell</td>
<td>- maximum delay cell</td>
</tr>
<tr>
<td>- minimum delay cell</td>
<td>- minimum delay cell</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## Gate characteristics

<table>
<thead>
<tr>
<th>$I_{\text{leak}}$ [nA]</th>
<th>HVT</th>
<th>LVT</th>
<th>M-LVT</th>
<th>MVT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_{\text{in}} = 00$</td>
<td>41</td>
<td>58</td>
<td>58</td>
<td>46</td>
</tr>
<tr>
<td>$E_{\text{in}} = 01$</td>
<td>43</td>
<td>101</td>
<td>101</td>
<td>46</td>
</tr>
<tr>
<td>$E_{\text{in}} = 10$</td>
<td>37</td>
<td>89</td>
<td>89</td>
<td>84</td>
</tr>
<tr>
<td>$E_{\text{in}} = 11$</td>
<td>19</td>
<td>236</td>
<td>19</td>
<td>19</td>
</tr>
</tbody>
</table>

| $I_{\text{average}}$ | 35 nA | 121 nA | 67 nA | 48 nA |
| Delay ($t_d$)        | 71 ps | 53 ps  | 53 ps | 60 ps |

BPTM 65nm technology
4. Application of Mixed-$V_{th}$
Design flow

- **HVT netlist**
  - estimate timing
  - find critical path
  - insert MLVT gates

- **MVT netlist**
  - estimate timing
  - estimate slack
  - insert HVT/MVT gates

New critical path

Slack changed
Slack

all Inputs of G1 arrived
all inputs of G2 arrived
G1 ready with evaluation
delay of G1
Slack for G1
MVT - Paths

Up to now: *two kinds of cells* (Dual-Threshold CMOS)

MVT-CMOS
MVT vs. LVT implementation

Reduction of Leakage

aver. 75%

96%

ISCAS Designs

c432  c499  c880  c1355  c1908  c2670  c3540  c5315  c6288  c7552
MVT vs. DVT implementation

![Reduction of Leakage]( ISCAS Designs)

- c432: 50%
- c499: 40%
- c880: 30%
- c1355: 20%
- c1908: 10%
- c2670: 0%
- c3540: aver. 27%
- c5315: 10%
- c6288: 0%
- c7552: 0%
5. Conclusion

- Subthreshold current $I_{sub}$ dominates leakage power
- Variation of $V_{th}$ affects $I_{sub}$ and delay
- Mixed-$V_{th}$ (MVT) combines advantages of DTCMOS at gate and at transistor level
- New gate type without additional masks in contrast to DTCMOS
- Average 75% (vs. LVT) and 27% (vs. DTCMOS) leakage reduction at constant delay
Thank you!

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