Mapping a Pipelined Data Path onto a Network-on-Chip

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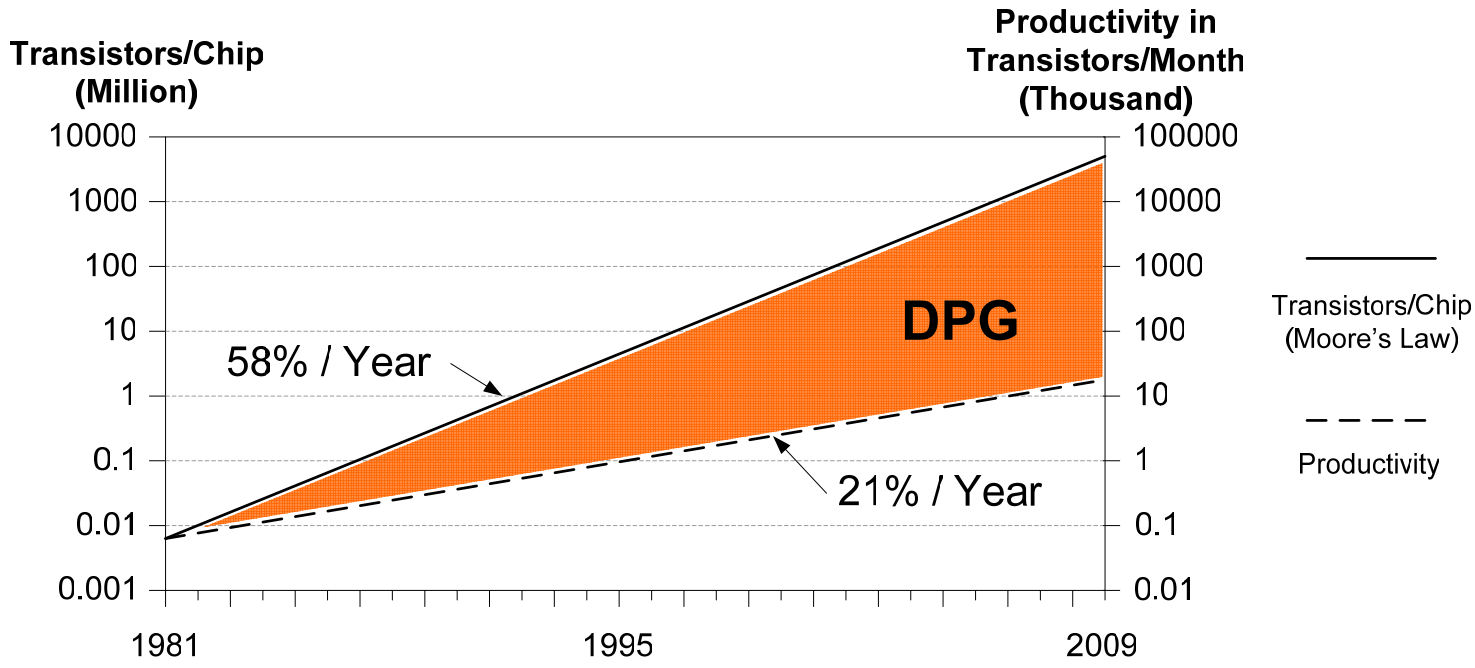
Outline

1. Introduction



Design-Productivity-Gap (DPG)

- Unbalanced development of integration density and productivity
- Current design flows cannot economically handle the large number of transistors

→ The goal is to cope with increasing complexity!

→ New approaches are needed, e.g., Networks-on-Chip [Dally,2001]

1. Introduction

Research Background

- Cooperation with Nokia Siemens Networks (formerly known as Siemens Networks)
  → Communications company
- Scenario: Ethernet-based access networks
- Protocols & new services
- Research on flexible & scalable hardware architectures for packet processing

Broadband Access Group

Location Greifswald, Germany

Goals of this Presentation

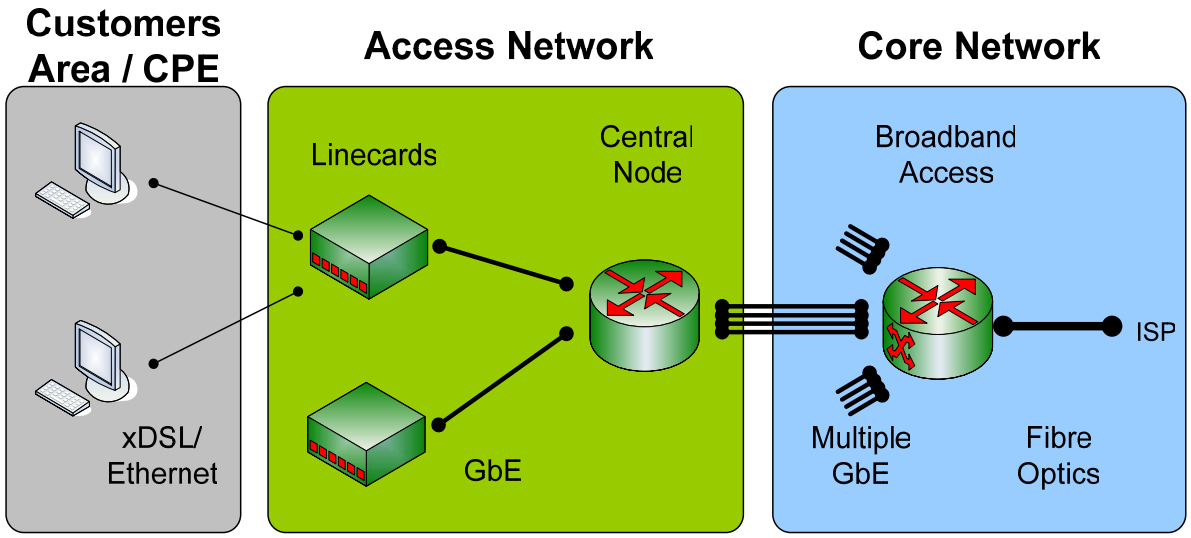
- …to introduce the application scenario and the redesigned system
- …to briefly introduce Networks-on-Chip as a new communication paradigm
- …to discuss the redesign process with focus on a Network-on-Chip architecture

Outline

2. Application Scenario

Access Networks – What is an Access Network???

- “Bridge” between subscribers (users) and ISPs (services)
- Aggregate & preprocess traffic in front of core networks
- Authentication/Authorization/Accounting of subscribers
- Current trends require architectural & algorithmic changes
  - → Increasing number of subscribers
  - → New technologies (xDSL, cable, fiber)
  - → More services (multi-media, triple & quadruple play)

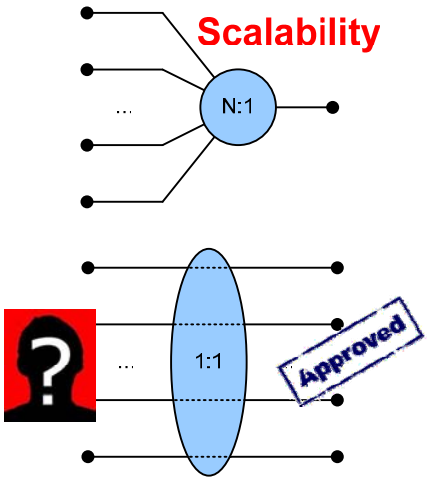


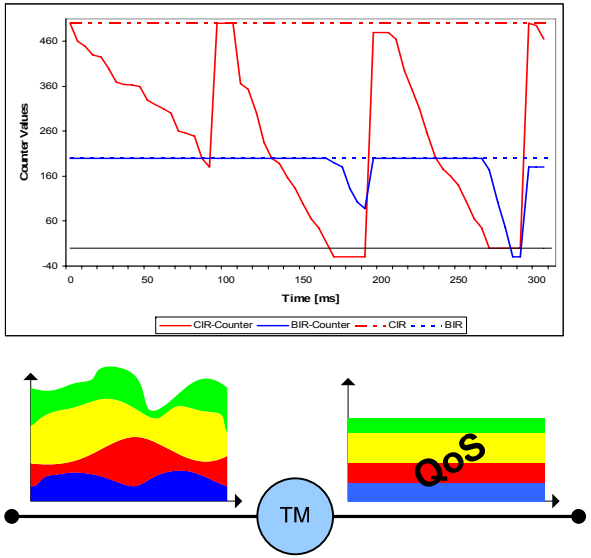
2. Application Scenario

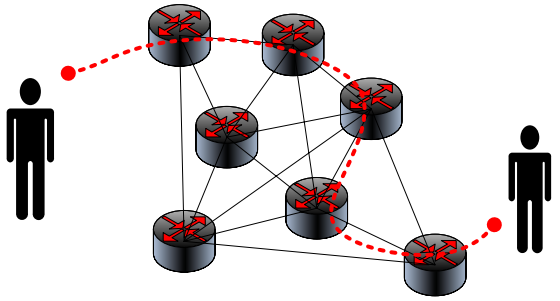
The MATMUNI System

- MAT : Layer 2 address translation → scalability & security
- TM : Metering, colormarking, policing → fair bandwidth scheduling
- MPLS-UNI : Extend MPLS towards the access network edges

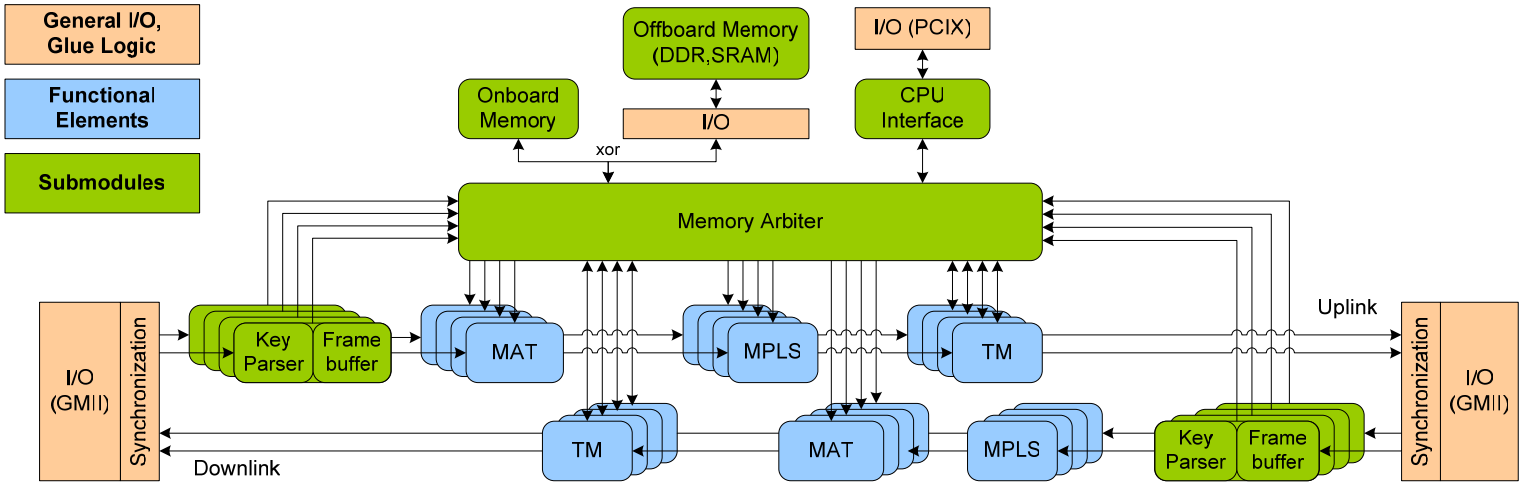
"sMAT – a simplified MAC Address Translation Scheme"
15th IEEE Workshop on Local and Metropolitan Area Networks (LANMAN), June 2007, Princeton, NJ, USA
"An integrated Hardware Solution for MAT, MPLS-UNI, and TM in Access Networks"
31st Annual IEEE Conference on Local Computer Networks (LCN), November 2006, Tampa, FL, USA
"Wirespeed MAC Address Translation and Traffic Management in Access Networks" & "A Simplified, Cost-Effective MPLS Labeling Architecture for Access Networks"
World Telecommunications Congress (WTC), April/May 2006, Budapest, Hungary







2. Application Scenario



MATMUNI's current Architecture

- Conventional approach, pipelined data path, signal-based communication
- Implemented on an FPGA (Xilinx Virtex-4)
- Designed for a specific scenario
  → Inflexible with respect to further extensions
  → Insufficient performance for future bandwidth demands
- Demands on a redesign / a new architecture
  → Scalable & flexible, low HW footprint, capacious bandwidth resources

Outline

3. Networks-on-Chip (NoCs)

Networks-on-Chip in general

NoCs are said to be a viable solution for the DPG and to handle complexity.

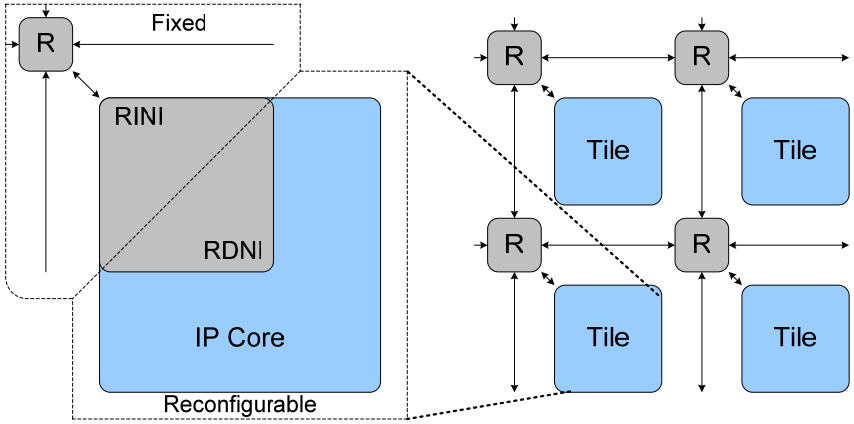
- On-chip interconnect infrastructure
- Long lines & busses replaced by parallel links
- Compliant to OSI reference model
- Influenced by the Internet & distributed systems
  → ≈ "Internet-on-Chip"
- IP cores with high modularity allow for high abstraction & reusability
- Packet-based communication separated from Computation

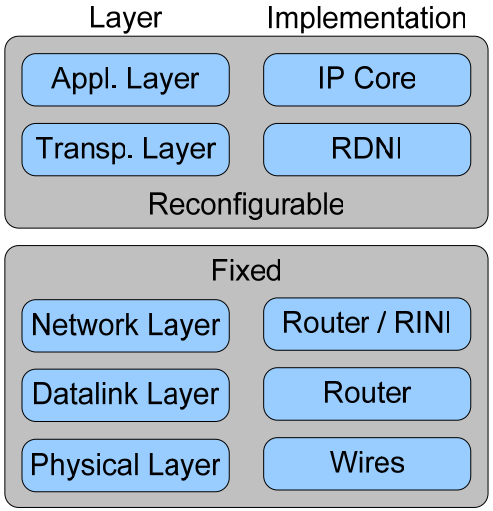
More general information needed?
http://www.networks-on-chip.com

3. Networks-on-Chip (NoCs)

Our own NoC

- Main building blocks: Routers (R), Links, IP cores (memory, CPUs, I/O)
- Resource-Network-Interfaces (RDNI/RINI)
- 2D-mesh topology, XY-routing
- Different switching types
- Layer 1-3 defined by the NoC
- Upper layers defined by application





Bandwidth Resources

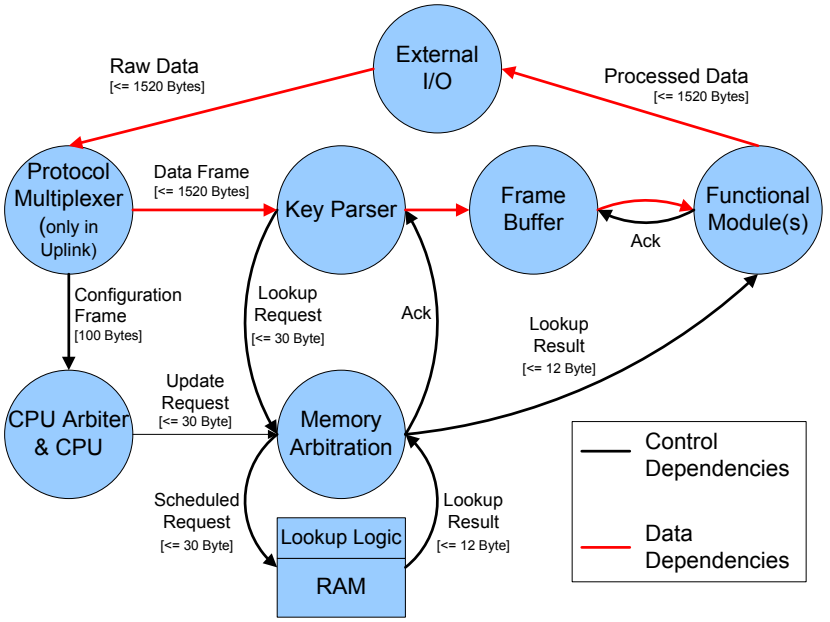
- Frequency 190–240 MHz (Xilinx Virtex-4 FPGA)
- One unidirectional link 3.84–6.88 Gbit/s (depending on the configuration)

Outline

4. Mapping MATMUNI onto the NoC – Analysis

Dependency Analysis of MATMUNI

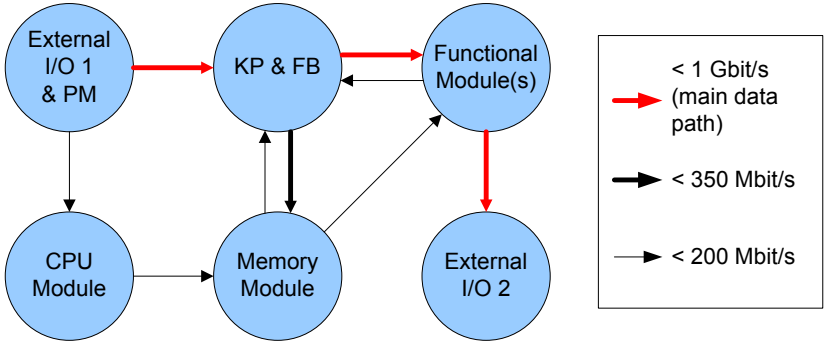
- APCG representation [Ogras, 2005]
- Communication dependencies between the entities
- MATMUNI:
  → Quite linear, one main data path
  → Vertical control dependencies
- Constant frame sequence, no reordering necessary



Bandwidth Requirements

- CTG representation [Ogras, 2005]
- Main data path = up to 1 Gbit/s
- Control paths = up to 350 Mbit/s

→ One NoC link offers up to 6.88 Gbit/s



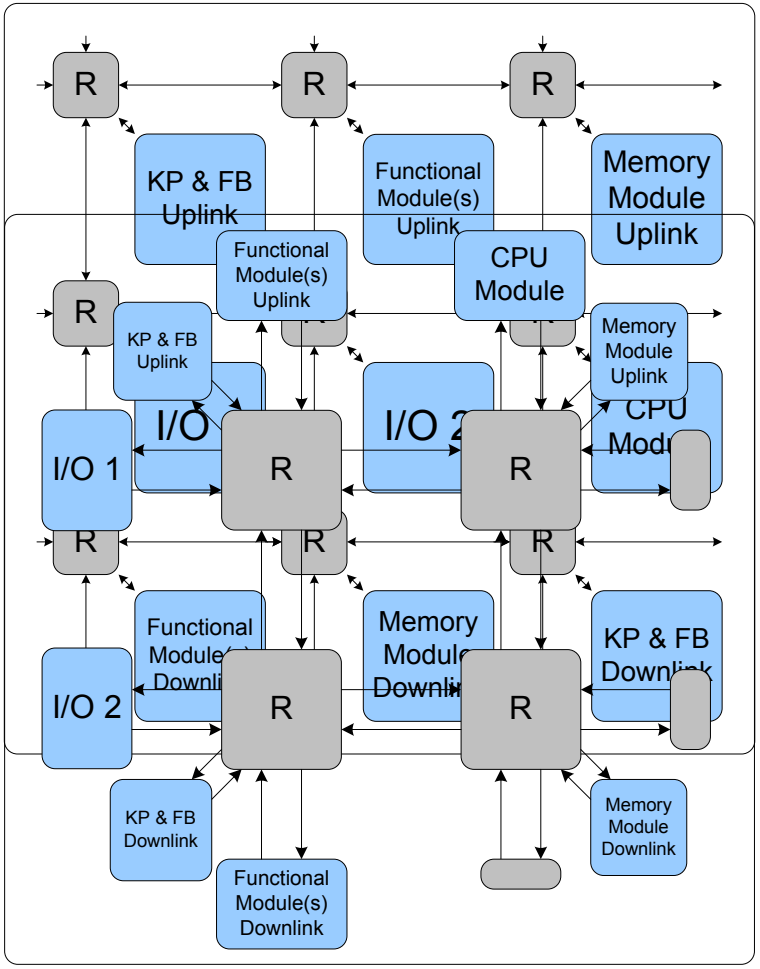
4. Mapping MATMUNI onto the NoC – Physical Mapping

Physical Mapping onto the NoC Grid

- Position of the logical entities in the NoC
- To be considered:
  - Location of hard-wired FPGA primitives
  - Dependencies between entities
  - Bandwidth requirements
- Goal: minimize link concurrency by efficient placement to exploit link bandwidth

Two different Mappings/Topologies

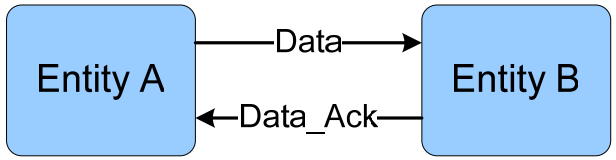
- Typical mapping with one IP core per router
  = Simple Routing, highly scalable
- Alternative mapping with fewer routers
  = Lower hw footprint, better utilization
- In either case → Separation of communication and computation!

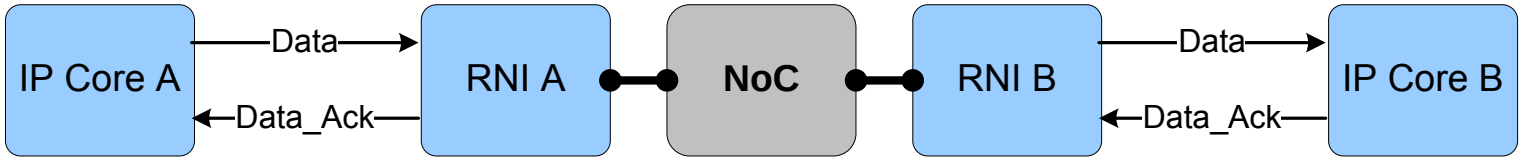


4. Mapping MATMUNI onto the NoC – Communication

Different Communication Paradigms

- Redesign requires a change in the communication paradigm
  → signal-based communication to message based communication
  → synchronous to asynchronous
- Constraints: constant frame order & no information loss

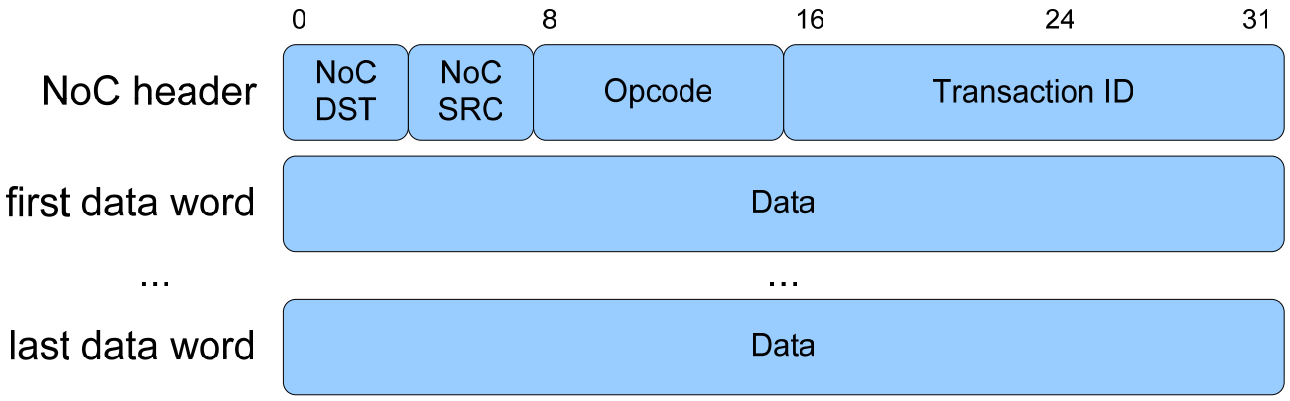




4. Mapping MATMUNI onto the NoC – Protocol

NoC-Protocol Development

- Special NoC protocol for MATMUNI
- Opcodes for different message types
  → Data (e.g., Ethernet frames, memory lookup results)
  → Control (e.g., lookup requests, signaling, exceptions)
- Assignment of transaction IDs on a per-frame basis
- Implemented in the NoC interface modules
  → Compliant to the layered protocol stack

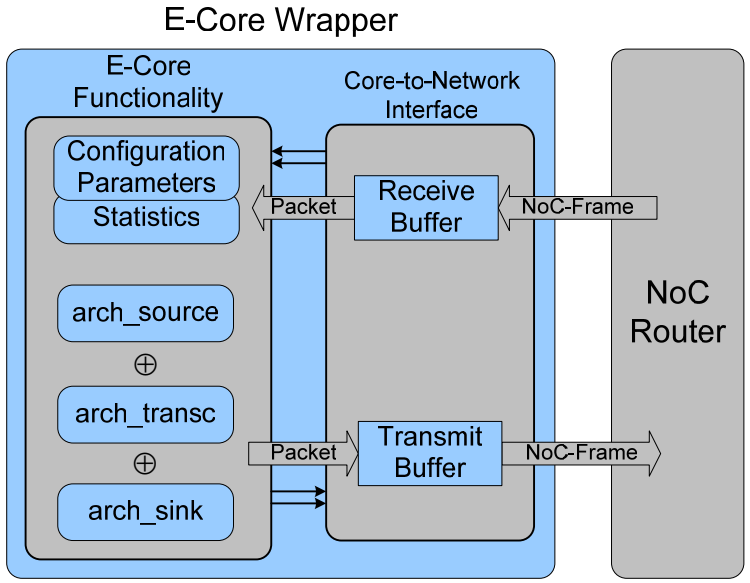


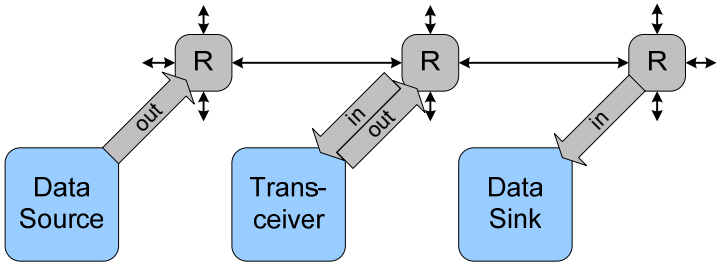
4. Mapping MATMUNI onto the NoC – Simulation

Simulation with E-Core

- E-Core? = VHDL emulation IP core
- Emulates typical behaviour of IP cores
  → Data source
  → Data sink
  → Transceiver
- Especially for packet processing and streaming media …
- Simulation without implementation of the functionality
- Adjustable to the constraints of each communication pair

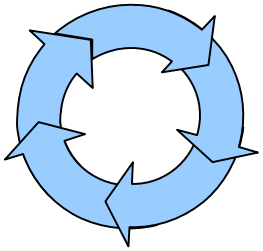
"E-Core - A Configurable IP Core for Application-specific NoC Performance Evaluation"
DATE'07, Workshop on Diagnostic Services in Network-on-Chips, Nice, France, April 16 - 20, 2007



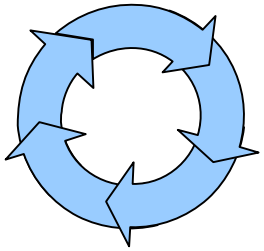


Outline

6. Summary



1. Different steps of the redesign of a packet processing system for a NoC architecture
2. Simple & efficient NoC infrastructure developed
3. NoCs are a viable solution for next generation integrated systems & systems-on-chip
    1. High abstraction & reusability
    2. Communication vs. computation
4. Next steps
    - Implementation of the last Resource-Network-Interfaces
    - Simulation of the entire NoC-based system
    - Setup for the FPGA board & in-field test



Thank you! Any questions?

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www.networks-on-chip.com