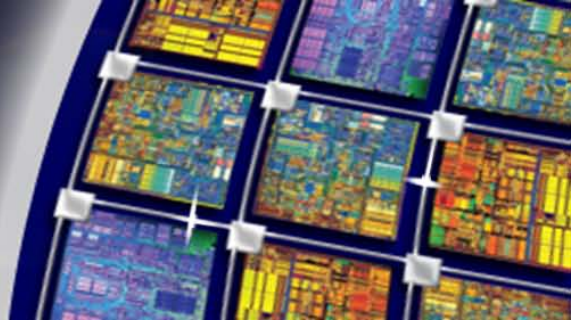

Monitoring and Control of Temperature in Networks-on-Chip

Tim Wegner, Claas Cornelius, Andreas Tockhorn, Dirk Timmermann;

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University of Rostock
Institute of Applied Microelectronics and Computer Engineering

Monitoring and Control of Temperature in NoCs

Outline

1. **Introduction**
2. Networks-on-Chip (NoCs)
3. Impact of Temperature on Reliability
4. Monitoring & Control of Temperature in NoCs
5. Summary

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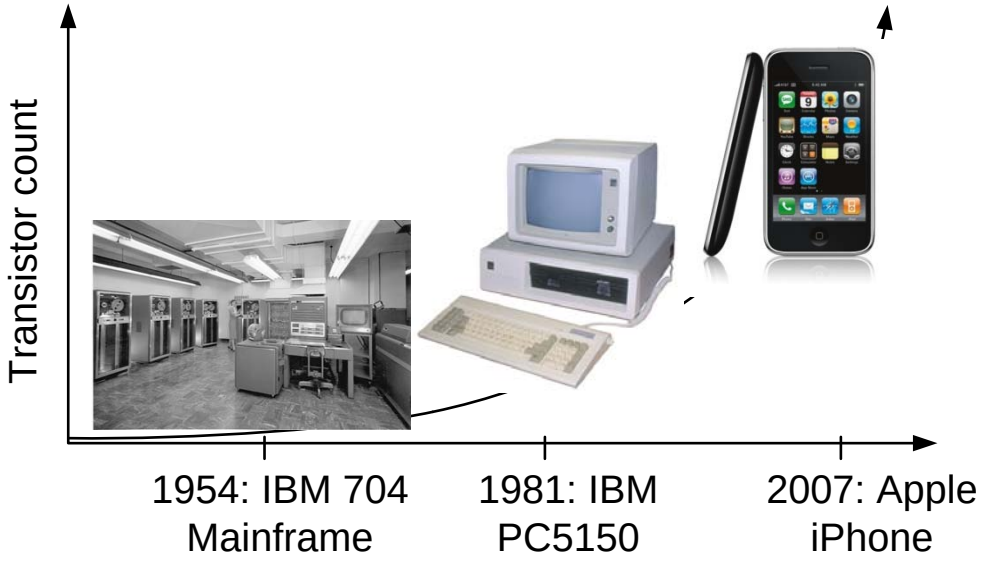
1. Introduction



Impacts of technological development

- Increasing integration density → rising complexity, shrinking device sizes

→ NoCs able to deal with arising requirements (e.g. for communication)

- But: Reliability becomes a dominant factor for chip design

→ Goal: Increase reliability in NoC-based systems

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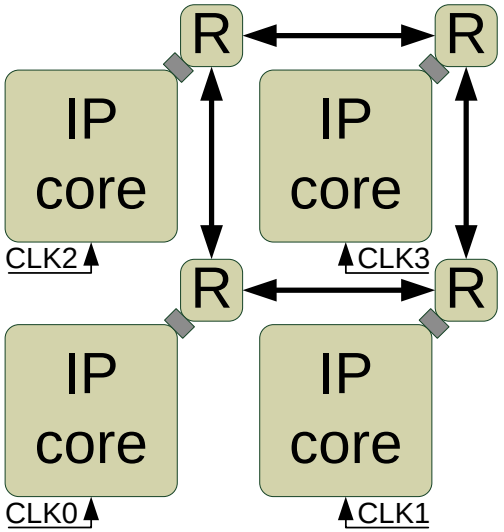
2. Networks-on-Chip

Properties

- Infrastructure for on-chip interconnection
- Point-to-point links replace long global busses
- Parallel packet-based communication
- Separation of communication & computation
- Globally asynchronous locally synchronous (GALS)
- Modularity of IP cores (not part of actual NoC)

→ reusability, high abstraction level



→ NoCs are able to satisfy requirements of modern VLSI systems

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3. Impact of Temperature on Reliability

Impacts of technological progress

- Increasing integration densities, progress of nanotechnology
  - → Growing number of transistors per chip = raised probability of failure
  - → decreasing structural size of ICs = higher susceptibility to environmental influences & deterioration

Intel 8086 (1978):
≈879 transistors/mm²

Intel Bloomfield (2008):
≈2,78 Mio. transistors/mm²

3. Impact of Temperature on Reliability

Why is thermal awareness important?

- Particular physical effects (e.g. TDDB, EM) contribute to deterioration
  → Abetted by high temperatures
- Correlation between temperature & failure mechanisms established by Arrhenius model
  → Exponential decrease of IC lifetime with temperature

$$T_{fail} \propto e^{\frac{E_a}{k_b * T}}$$

→ Growing influence of on-chip temperature distribution on lifetime, operability, performance etc.

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4. Monitoring and Control of Temperature for NoCs

Objective:

- Mitigate effects contributing to deterioration & delay occurrence of failures
  → Control of on-chip temperature distribution

Requirements:

☑ Effective mechanisms to monitor & control on-chip temperature
☑ Integration into existing NoC
- Preservation of modularity & reusability
- Minimum costs (area, frequency)
- Maximum performance of monitoring and control
- Minimum impact on system performance

4.1 Mechanisms for monitoring

- Concept: attach physical monitoring probes to every IP core

Event-driven:

- temperature variation ΔT
- Continuous checking of T_{IPC}
- $|T_{IPC,old} - T_{IPC,new}| \geq \Delta T$?

$\rightarrow$ Report $T_{IPC,new}$

- Area: 66 LUT/FF pairs
- Frequency: 227 MHz

Time-driven:

- Period of time Δt

$\rightarrow$ Report $T_{IPC,new}$ every Δt

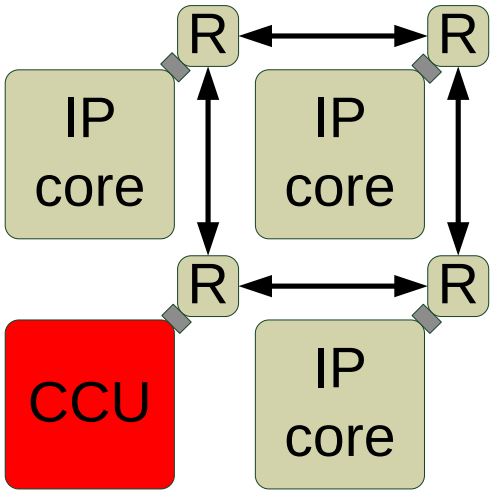
- Area: 80 LUT/FF pairs
- Frequency: 338 MHz

4.2 Mechanisms for control

Central Control Unit (CCU):

- Reception & interpretation of probe packets
- Instructions for Dynamic Frequency Scaling to probes (if necessary)

- Area: 507 LUT/FF pairs
- Frequency: 165 MHz



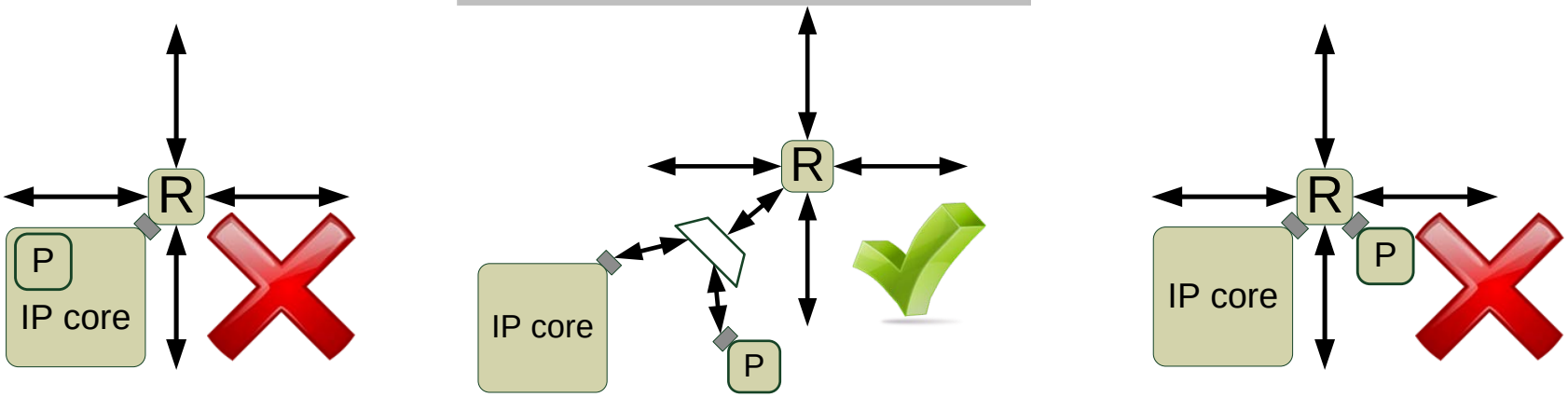
!!! Not the smartest approach, but suffices to test functionality !!!

4.3 Integration of monitoring

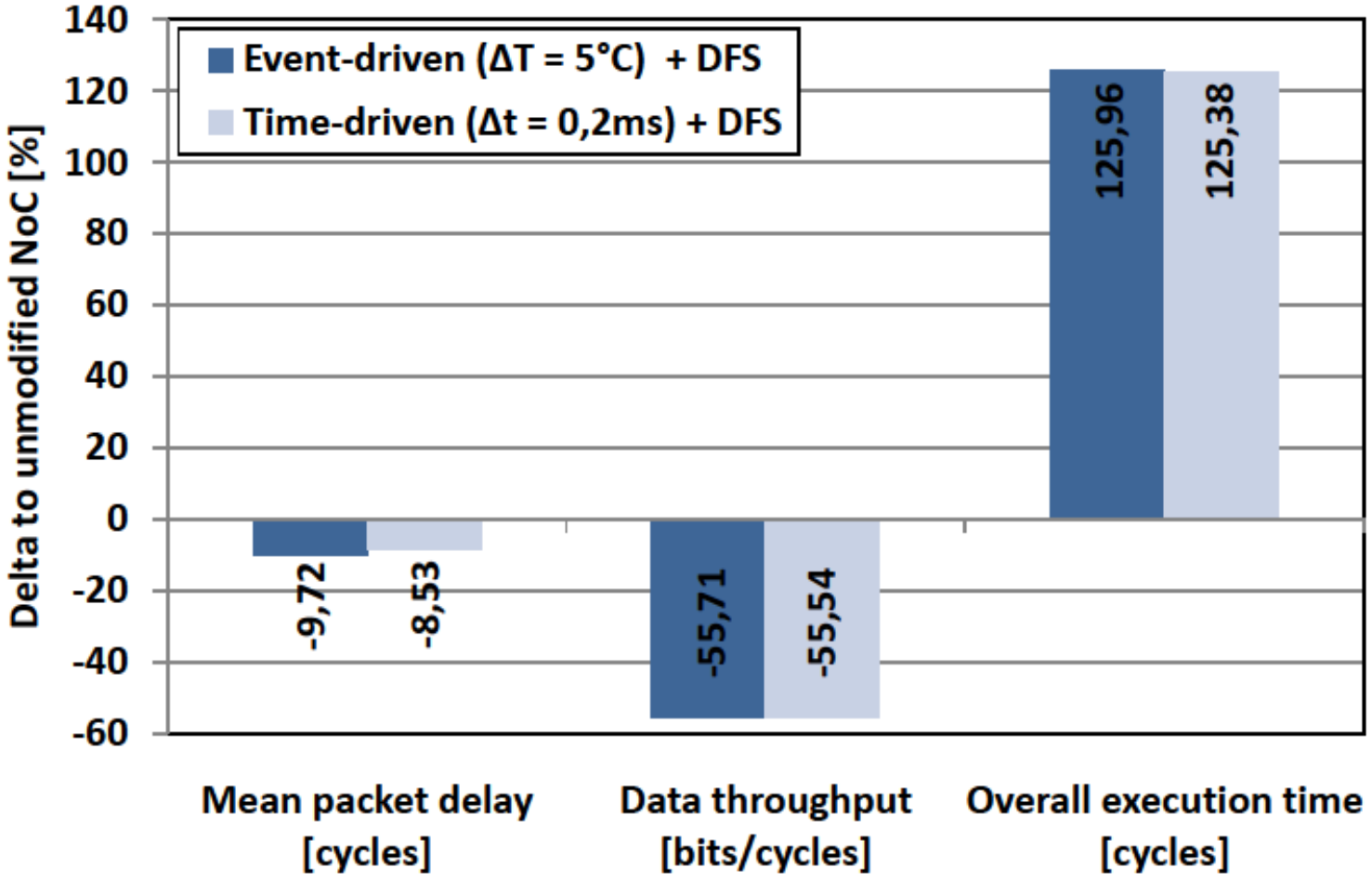
- 3 approaches

→ Different impact on performance & costs

Into IP core:	Router port of IP core:	Extra router port:
▪ Area penalty: / ▪ Freq. penalty: /	▪ Area penalty: 7,3% ▪ Freq. penalty: / (but Mux/Demux)	▪ Area penalty: 30,5% ▪ Freq. penalty: 8,2%

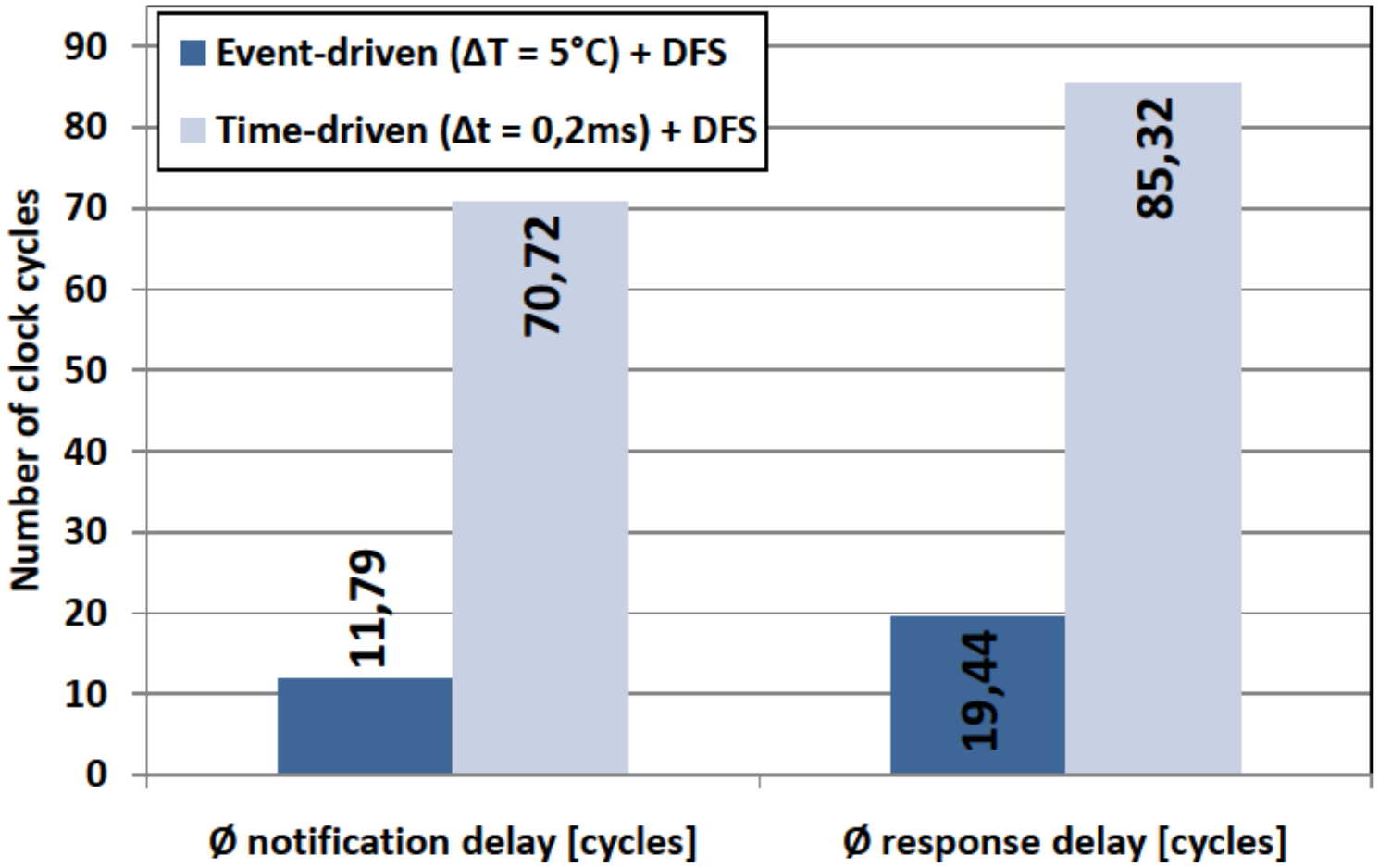


4.4 Impact on system performance



Monitoring and Control of Temperature in NoCs

4.5 Performance of monitoring & control



Monitoring and Control of Temperature in NoCs

5. Summary

- Implementation of 2 approaches for monitoring on-chip temperature + 3 methods for integration into NoC

→ Investigation of:

- Costs (area, frequency)
- Impact on system performance
- Performance of monitoring & control

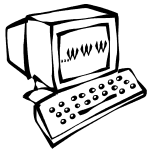
Conclusion

- Event-driven approach preferable (situational monitoring, better performance, no redundant traffic, lower area costs)
- Integration into NoC using router port of IP core best trade-off between costs & preservation of modularity/non-intrusiveness

Thanks for your attention!
Any questions?

Contact: tim.wegner@uni-rostock.de

Homepage: www.networks-on-chip.com



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