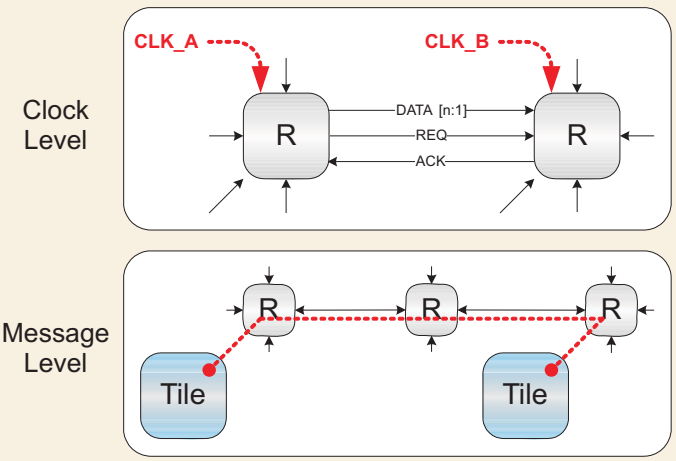
Network-on-Chip Communication Grids for High Performance Packet Processing

GALS on Different Levels



Application-specific NoC Design

A priori aspects & requirements of packet processing:

- Main data paths with streaming data (up-/downlink)
- Defined bandwidth constraints, e.g., Gbit Ethernet
- Non-blocking performance
- Internet is highly dynamic (workload, protocol stack)

Using a priori knowledge for:

- Function mapping & traffic engineering
- Channel width & buffer sizing
- Omit sophisticated QoS in the NoC infrastructure

→ A priori knowledge is **for free!**

Feature-rich platforms

We need:

- Independent clocks for GALS
- Buffer space for the NoC and clock domain crossing

FPGAs provide:

- Multiple clock nets
- PLLs & DCMs
- Plenty of memory resources (FIFOs, RAM blocks, registers)

→ Use is **for free!**

One Problem still remains!

Resource overhead of NoCs in FPGAs! NoCs consume valuable logic resources.

Two arguments against:

1.) Moore's Law is also true for FPGAs
- Resource overhead diminishes
- Principally, transistors are for free
  - ➡ But costly when connected

2.) NoC is new paradigm...
- ...and thus **not yet matured**
- NoCs will be matured in future ICs (as hardwired macro or in logic)

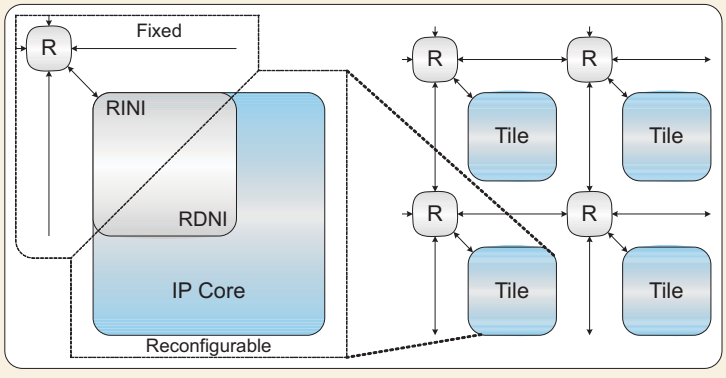
What do we gain?

- Handling complexity by "Devide-and-conquer" approach
- Scalability
- IP reuse by modular design

- Performance of hardware
- Flexibility of software

- Feasible architecture for applications with high demands on performance
  - Networking & packet processing
  - Multimedia
  - Adaptive & autonomous systems
  - Partial dynamic reconfiguration

Network-on-Chip Communication Grid



- Simple NoC, used just as **wire replacement**
  - 2-dimensional XY Routing
  - Virtual-cut-through or wormhole switching
  - No priorities, round-robin
  - 32 Bit data width
- Shift QoS into higher (reconfigurable) layers

Version	f [MHz]	Register	Block RAM	LUTs	Link BW [Gbit/s]
Wormhole	193	315	-	925	6.17
Virtual-cut-through	215	225	5	1117	6.68

SYNPLIFY PRO SYNTHESIS (VIRTEX4 FX20)

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