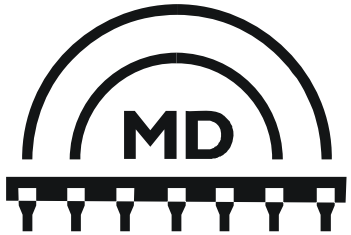
A Mesochronous Network-on-Chip for an FPGA

Stephan Kubisch, Enrico Heinrich, Dirk Timmermann

{stephan.kubisch;enrico.heinrich;dirk.timmermann}@uni-rostock.de

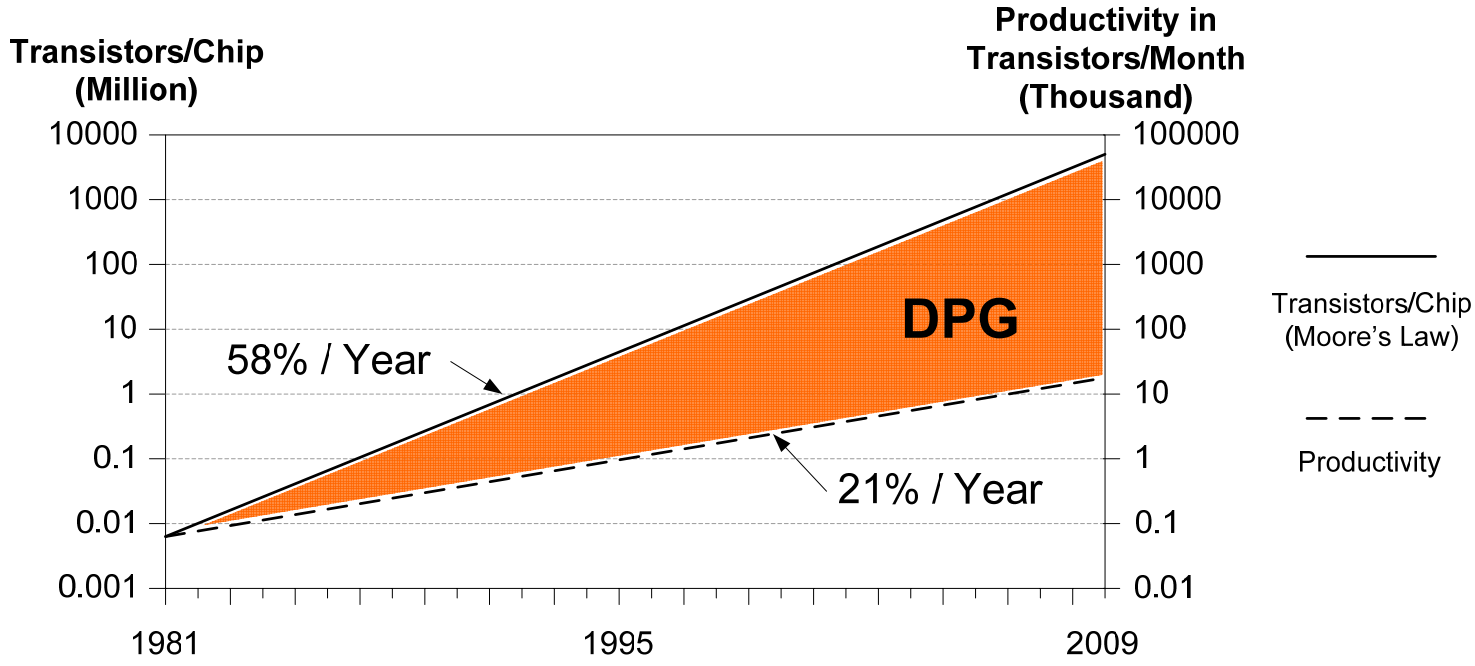
University of Rostock
Institute of Applied Microelectronics and Computer Engineering



MEMICS 2007, Znojmo, Czechia, October 26-28

Outline

1. Introduction



Design-Productivity-Gap (DPG)

- Unbalanced development of integration density and productivity
- Current design flows cannot economically handle the complexity

→ The goal is to cope with increasing complexity!

→ New approaches are needed, e.g., Networks-on-Chip & GALS

Outline

2. Networks-on-Chip

Networks-on-Chip in general

NoCs are said to be a viable solution for the DPG and to handle complexity.

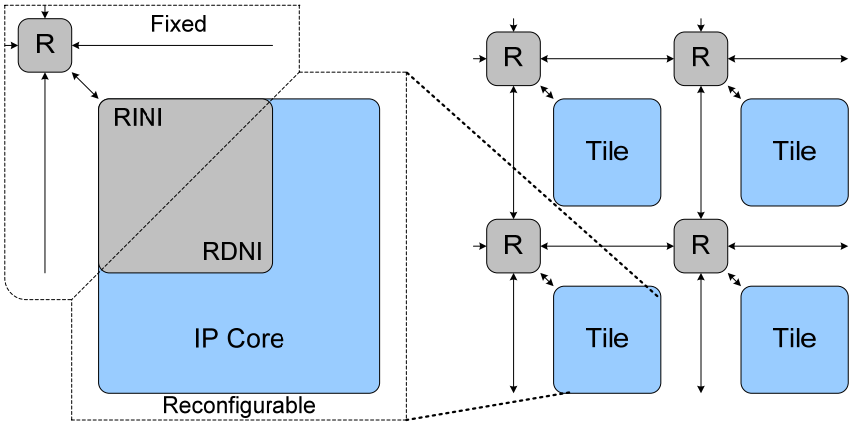
- On-chip interconnect infrastructure
- Long lines & busses replaced by parallel links
- Compliant to OSI reference model
- high modularity using IP cores
  → High abstraction & reusability
- Packet-based asynchronous communication
- Communication separated from computation

More general information needed?
http://www.networks-on-chip.com

2. Networks-on-Chip

Our own NoC

- Main building blocks:
  routers (R), links, resource-network-interfaces (RDNI/RINI)
- 2D-mesh topology, XY-routing
- Different switching types
- IP cores contain the functionality and do not belong to the literal NoC



Starting Point: synchronous NoC

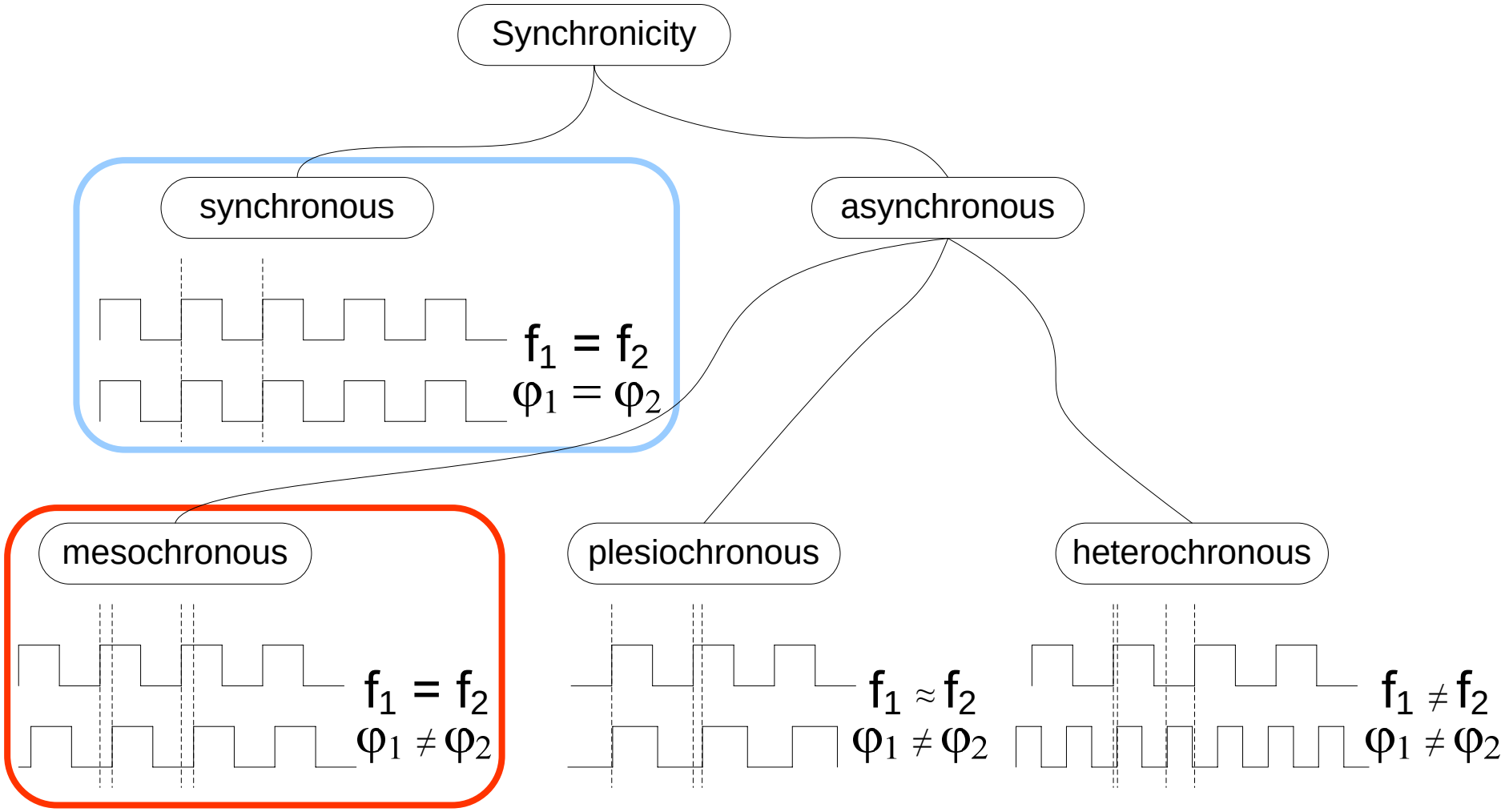
Problem:
Frequency = function of NoC size

What do we want? – Scalability!

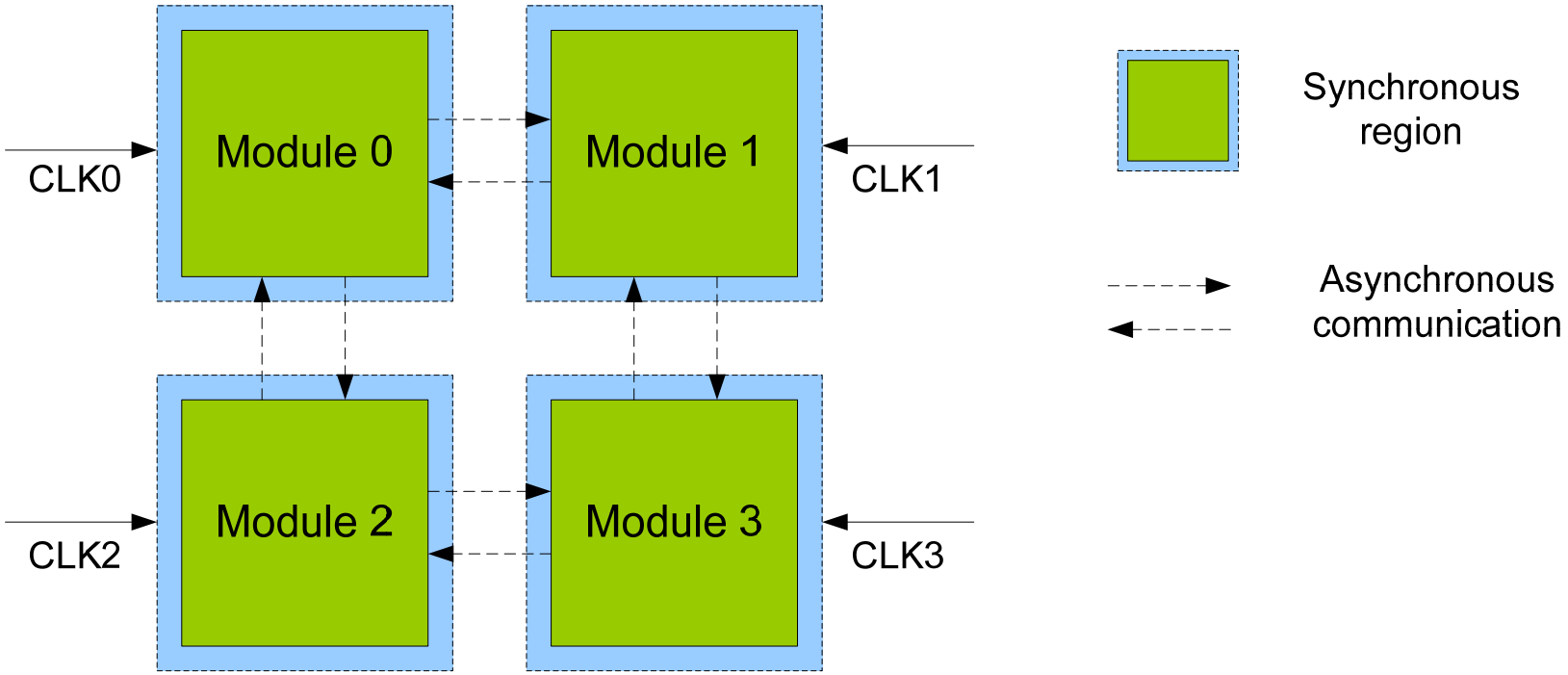
Frequency = function of a single NoC router's complexity

Outline

3. GALS – Flavors of Synchronicity

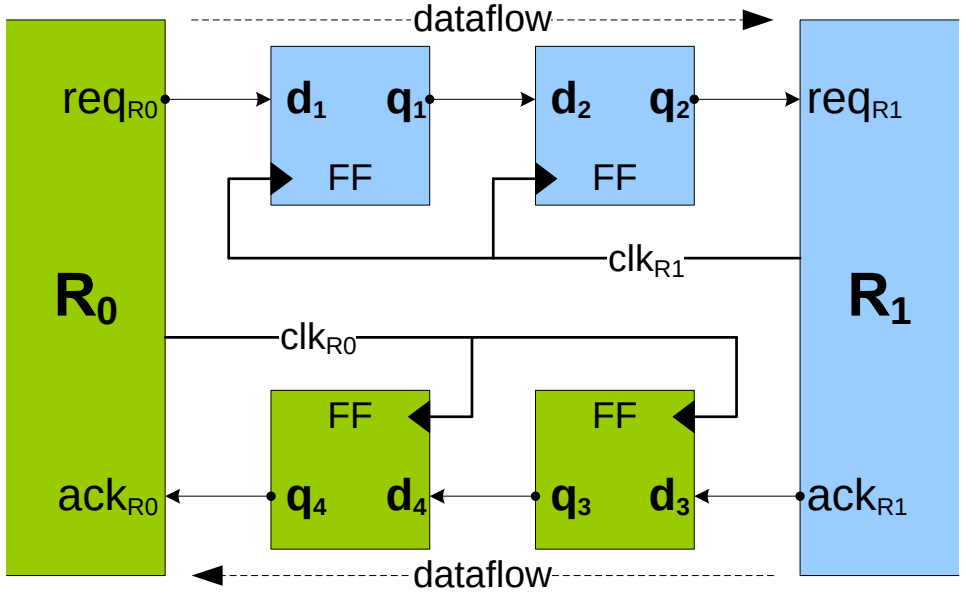


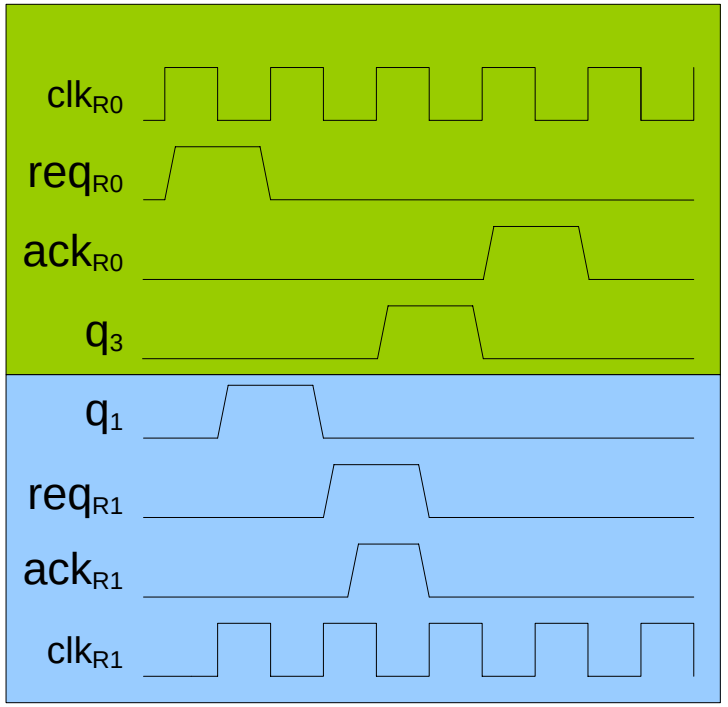
3. GALS – Design Structure



- Typical GALS structure
- Similarities with Network-on-Chip structure

3. GALS – Clock Domain Crossing





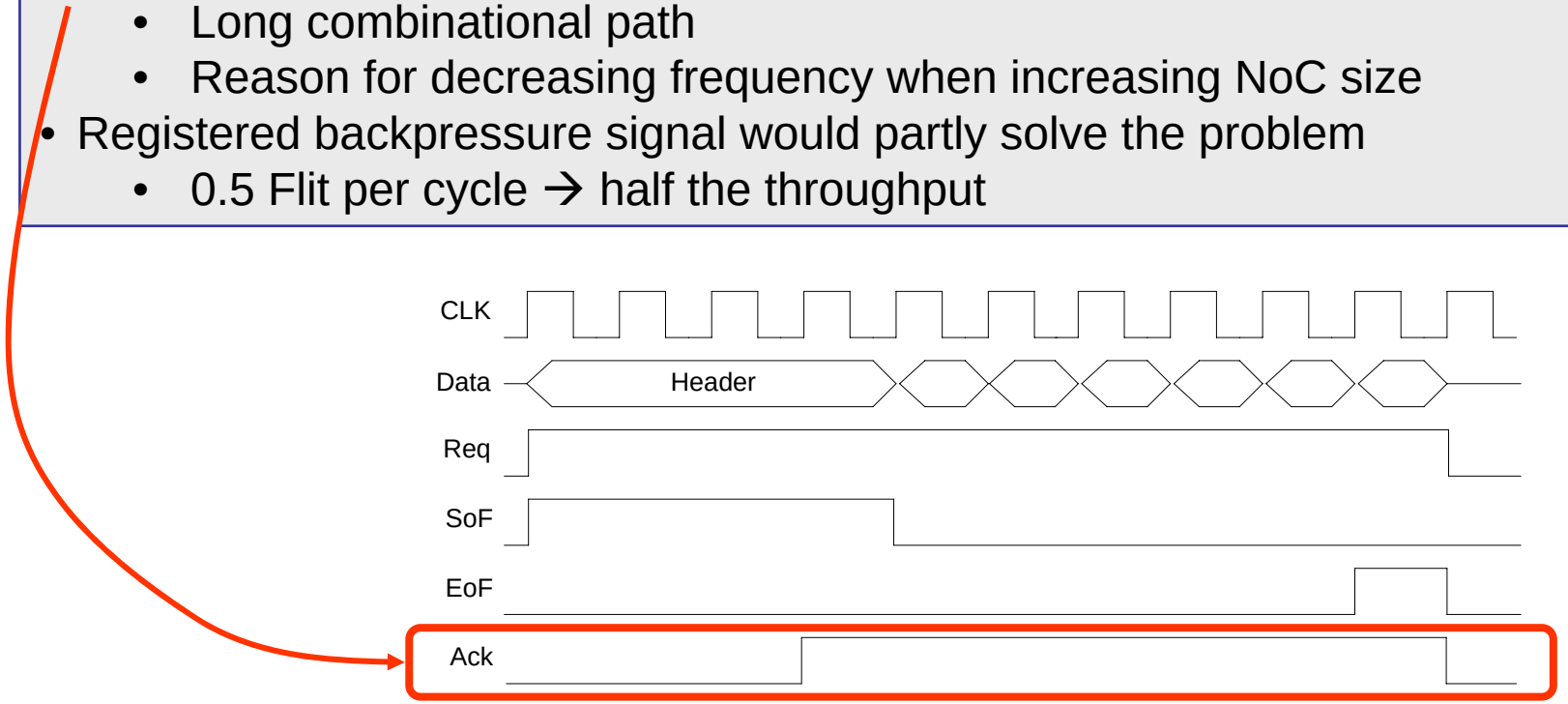
- simple Two-FF-Synchronizer used in our NoC design

Outline

4. The Mesochronous NoC

Starting Point: Synchronous Wormhole Switching

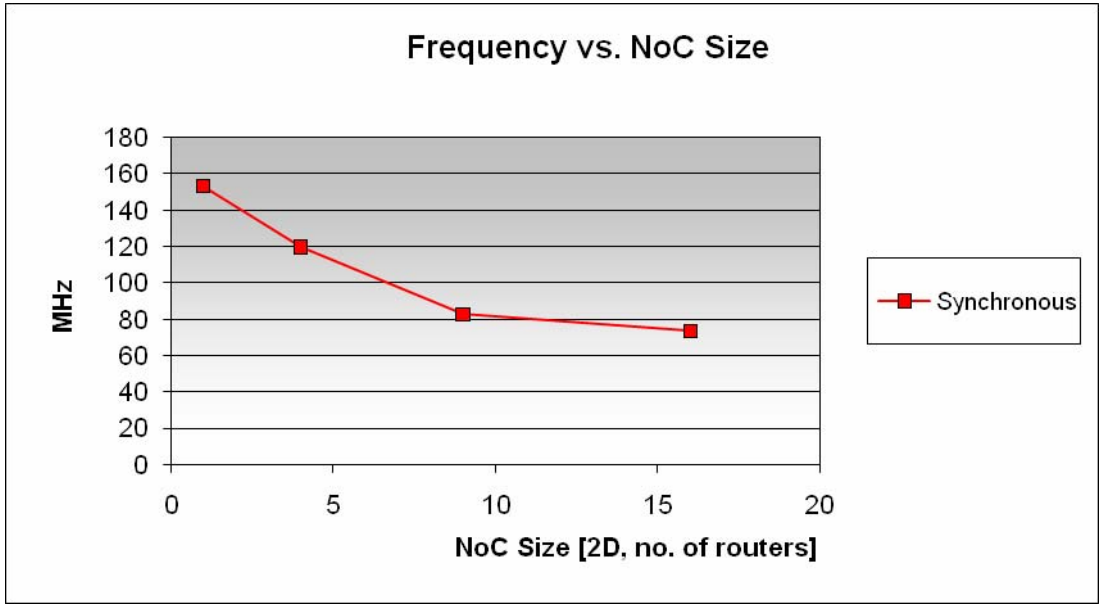
- 1 Flit per cycle → **high average throughput**
- Buffer for 1 flit per port → **minimal hardware overhead**
- But! combinational backpressure signal, every flit is ack'ed
  - Long combinational path
  - Reason for decreasing frequency when increasing NoC size
- Registered backpressure signal would partly solve the problem
  - 0.5 Flit per cycle → half the throughput



4. The Mesochronous NoC

Goal & Constraints

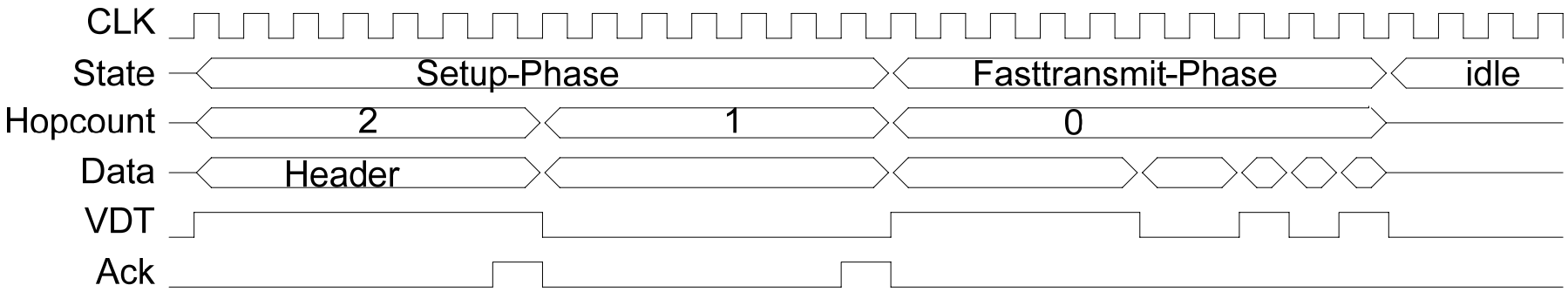
- Goal: *frequency depends only on NoC router*
- Constraints:
  - Reasonable hardware overhead
  - Minimal performance loss



4. The Mesochronous NoC

New Mesochronous Wormhole Switching

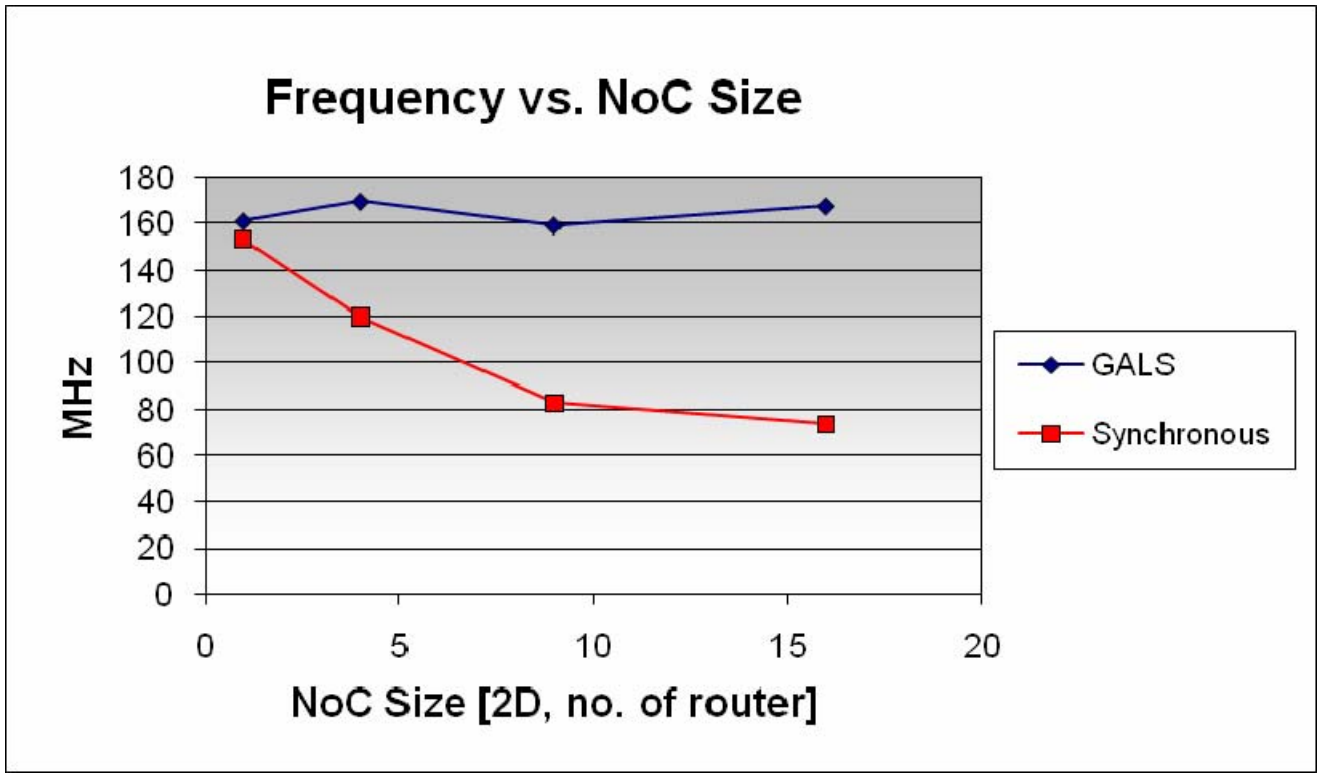
- HSM – Hybrid Switching Mechanism
- Two phases:
  - Setup phase – define the route through the NoC
  - Fast transmit phase – route established, 1 flit per Cycle
- Additional delay during setup phase due to clock domain crossing
- Throughput similar to synchronous wormhole switching (for long packets)
- Deterministic routing algorithm strictly required



4. The Mesochronous NoC

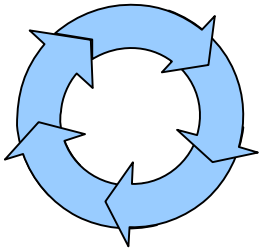
- Synchronous: max. frequency depends on total NoC size
- Mesochronous: max. frequency depends only on router size

→ Bandwidth & throughput much higher due to stable max. frequency



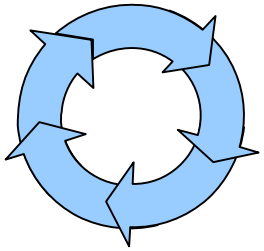
Outline

5. Summary



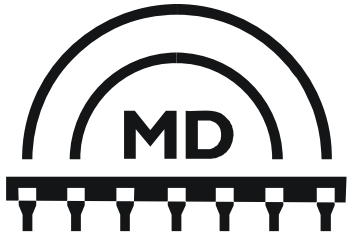
- NoCs are a viable solution for next generation integrated systems & systems-on-chip
  - High abstraction & reusability
  - Communication vs. computation
- A simple & efficient mesochronous NoC infrastructure has been developed
- Stable max. operation frequency
- Fast, resource-aware switching scheme

- Asynchronicity
  - On the clock level (GALS)
  - On the packet level (NoC communication)



Thank you! Any questions?

stephan.kubisch@uni-rostock.de
www.networks-on-chip.com



4. The Mesochronous NoC