Scalable VHDL Architectures for Non-Uniform Sampling Driver Design

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Overview

- Sampling driver (SD) design requirements
  - Realize constant sampling point density function
  - Avoid too small intersample times with respect to used ADC
  - Match SD system clock period and PDF of sampling instance
- Architecture and scalability
  - Top level view of a non-uniform sampling device
  - SD architecture
  - Detailed view of SD core
  - SD scalability

SD Design Requirements

1. Solution (straight forward)

- Realize a constant sampling point density function (SPDF)

Jittered random sampling (JRS). Sampling instance PDF matched to SD system clock period.

- SD system clock period T_{clk}
- Sampling instance $t_k(t)$
- Time quantum T_Q
- Clock period to time quantum ratio $M = T_{clk} / T_Q$
- Random number e_k

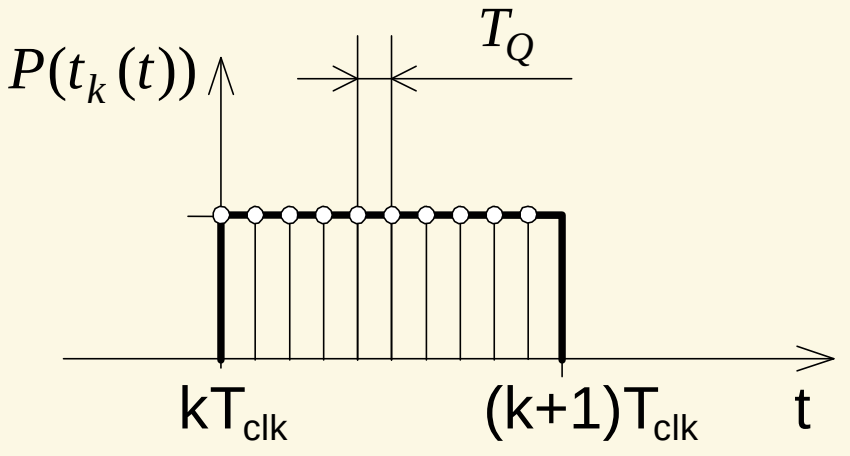
$$t_k = kT_{clk} + e_k T_Q$$

SD Design Requirements

1. Solution (straight forward)

- Realize a constant sampling point density function (SPDF)

PDF of sampling instance (JRS)

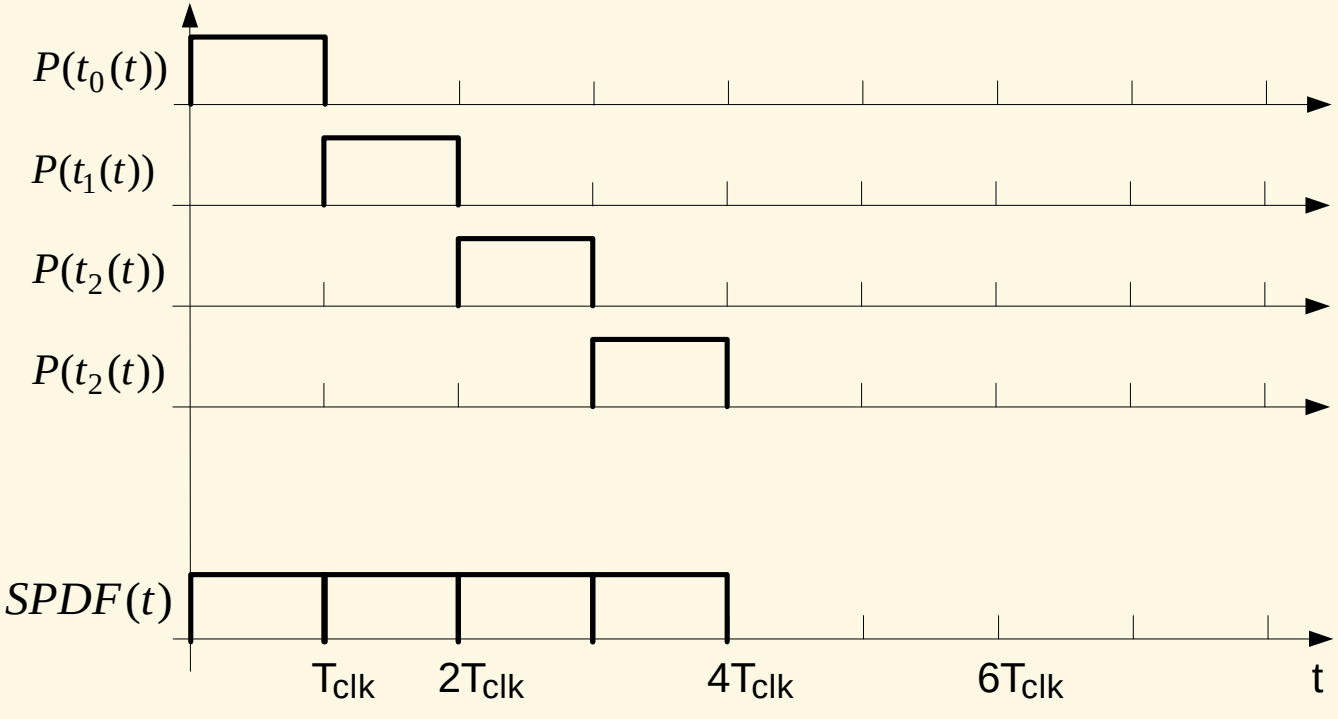


SD Design Requirements

1. Solution (straight forward)

- Realize a constant sampling point density function (SPDF) ✓

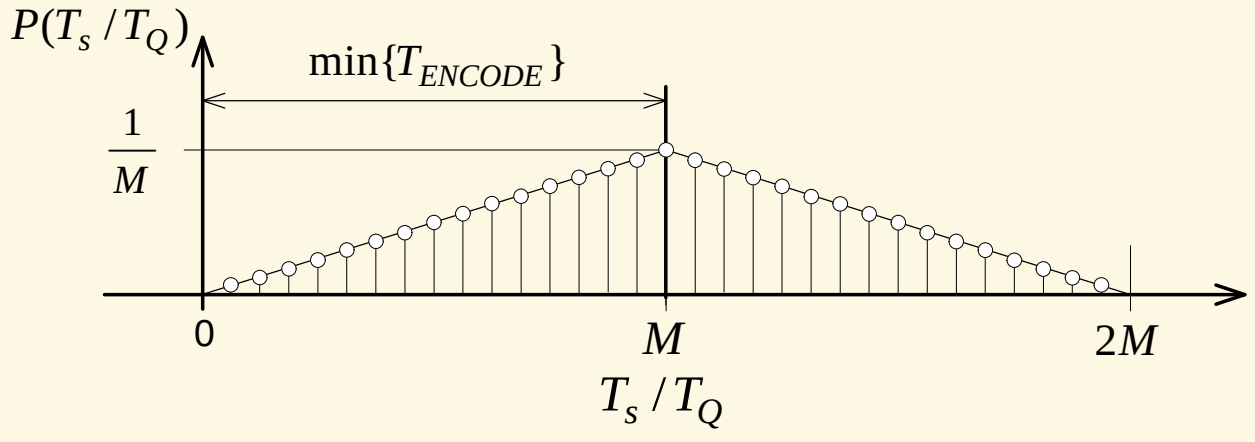
sampling point creation process



SD Design Requirements

1. Solution (straight forward)

- Realize a constant sampling point density function (SPDF) ✓
- Avoid too short intersample times —



→ Problem: 50% of intersampling times too short for ADC

SD Design Requirements

2. Solution (optimized)

- Realize a constant sampling point density function (SPDF)

Additive random sampling (ARS). Sampling instance PDF matched to SD system clock period.

- Deliberate phase shifts
- Corr(ε_k, ε_{k-1}) = 0.5

$$t_k = t_{k-1} - e_{k-1}T_Q + T_{clk} + \begin{cases} 0 & if \quad e_{k-1} < \frac{M}{2} \\ T_{clk} & otherwise \end{cases}$$

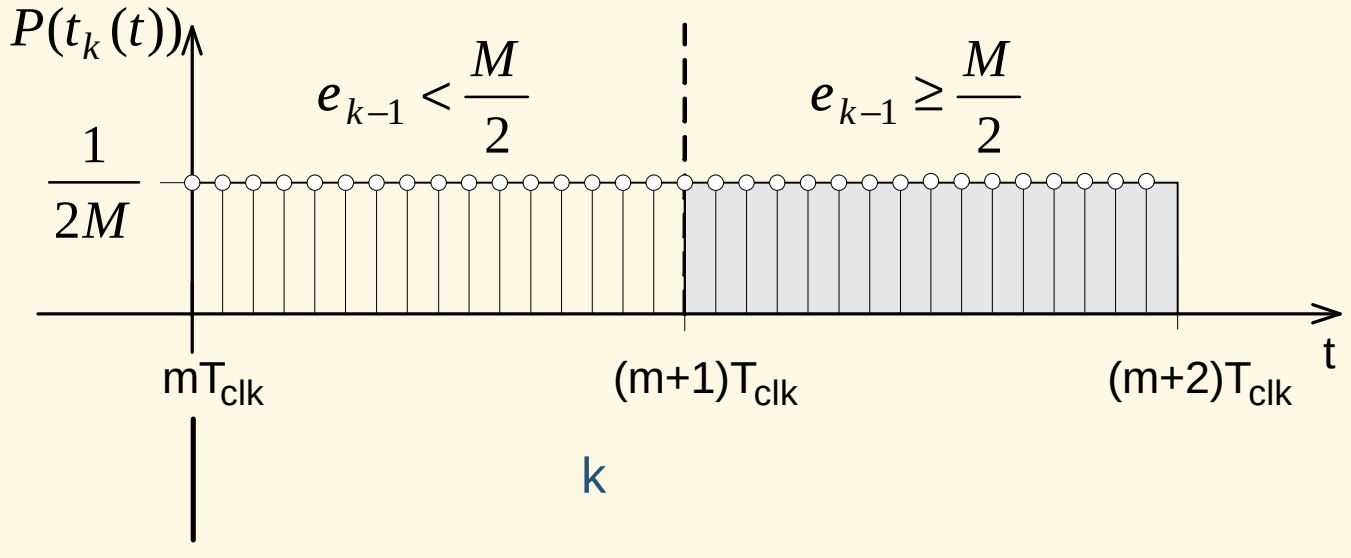
$$+ e_k T_Q$$

SD Design Requirements

2. Solution (optimized)

- Realize a constant sampling point density function (SPDF)

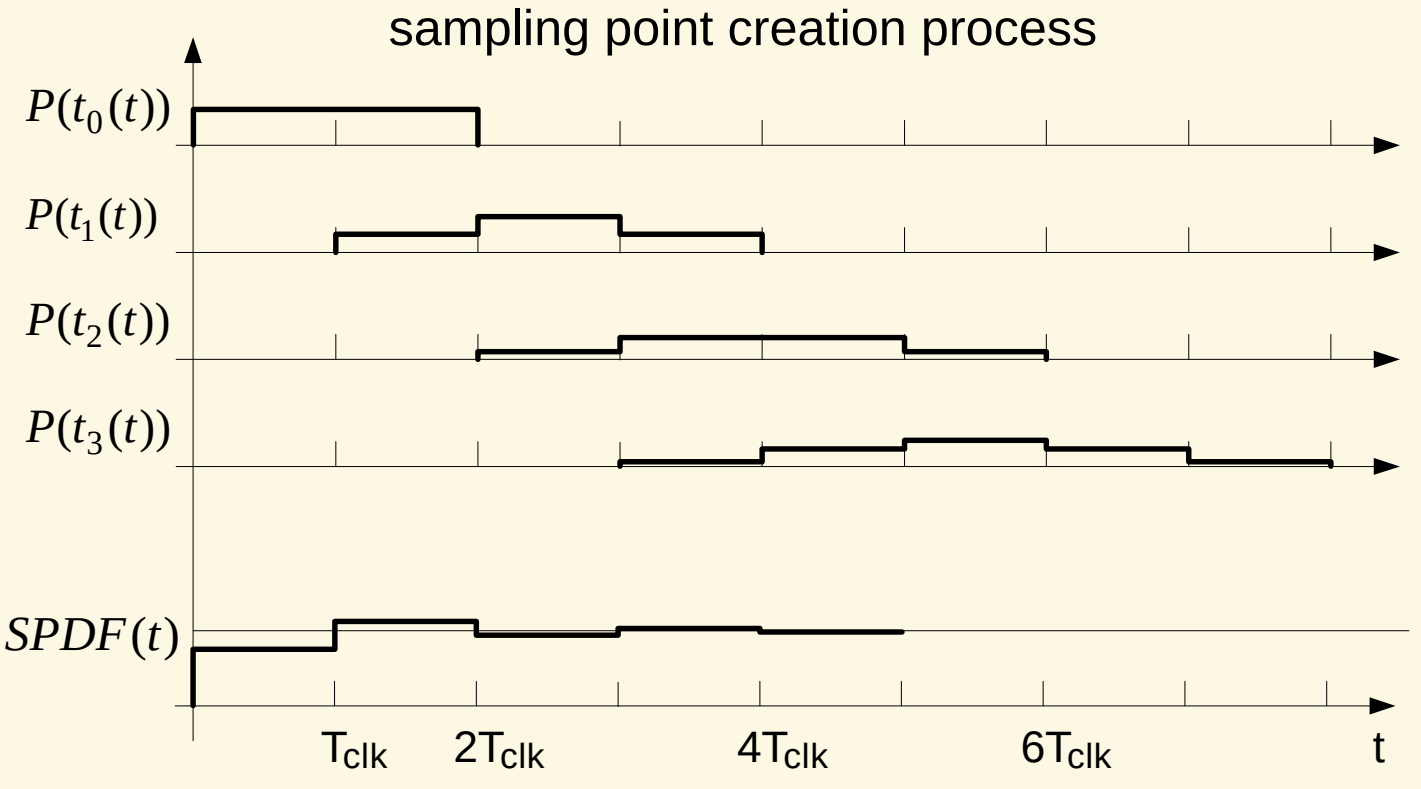
PDF of sampling instance (ARS)



SD Design Requirements

2. Solution (optimized)

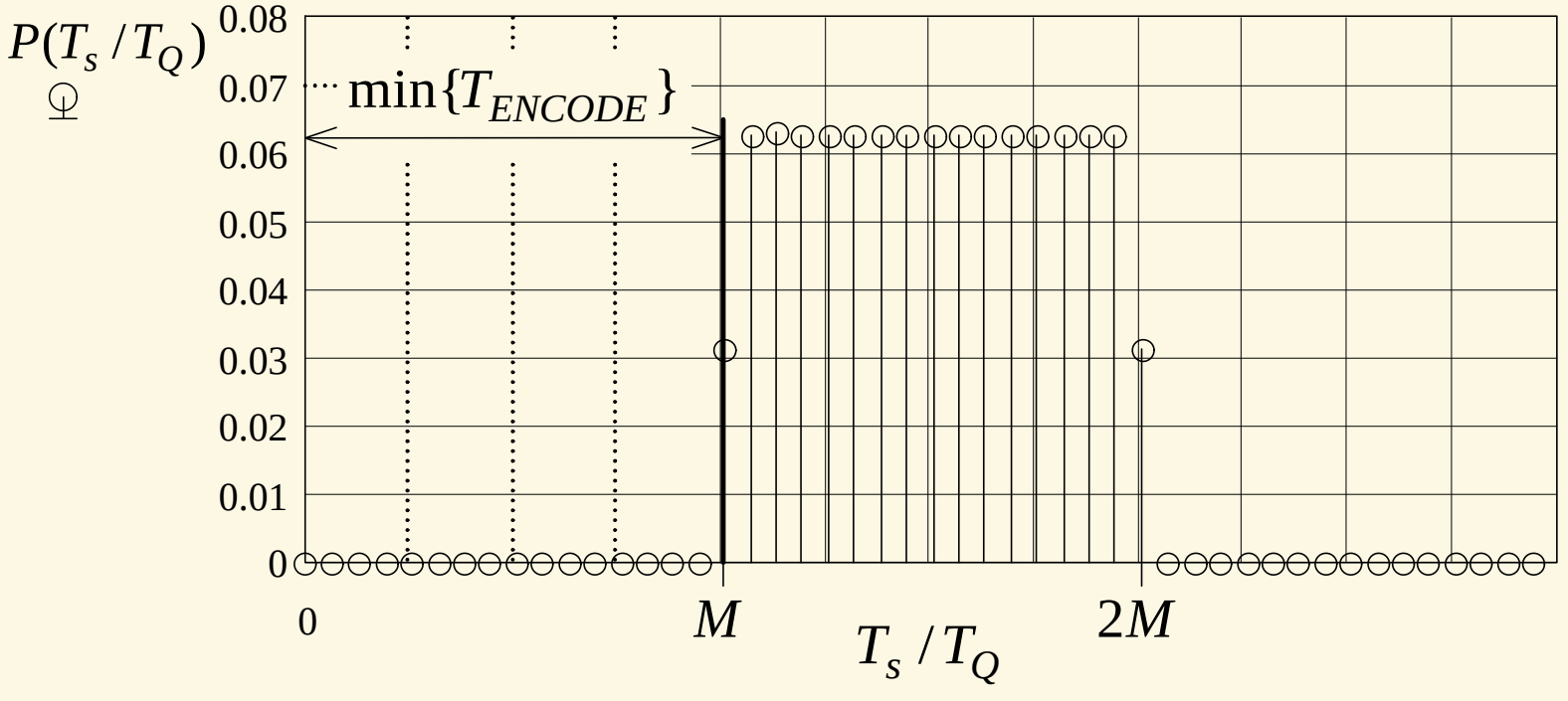
- Realize a constant sampling point density function (SPDF) ✓



SD Design Requirements

2. Solution (optimized)

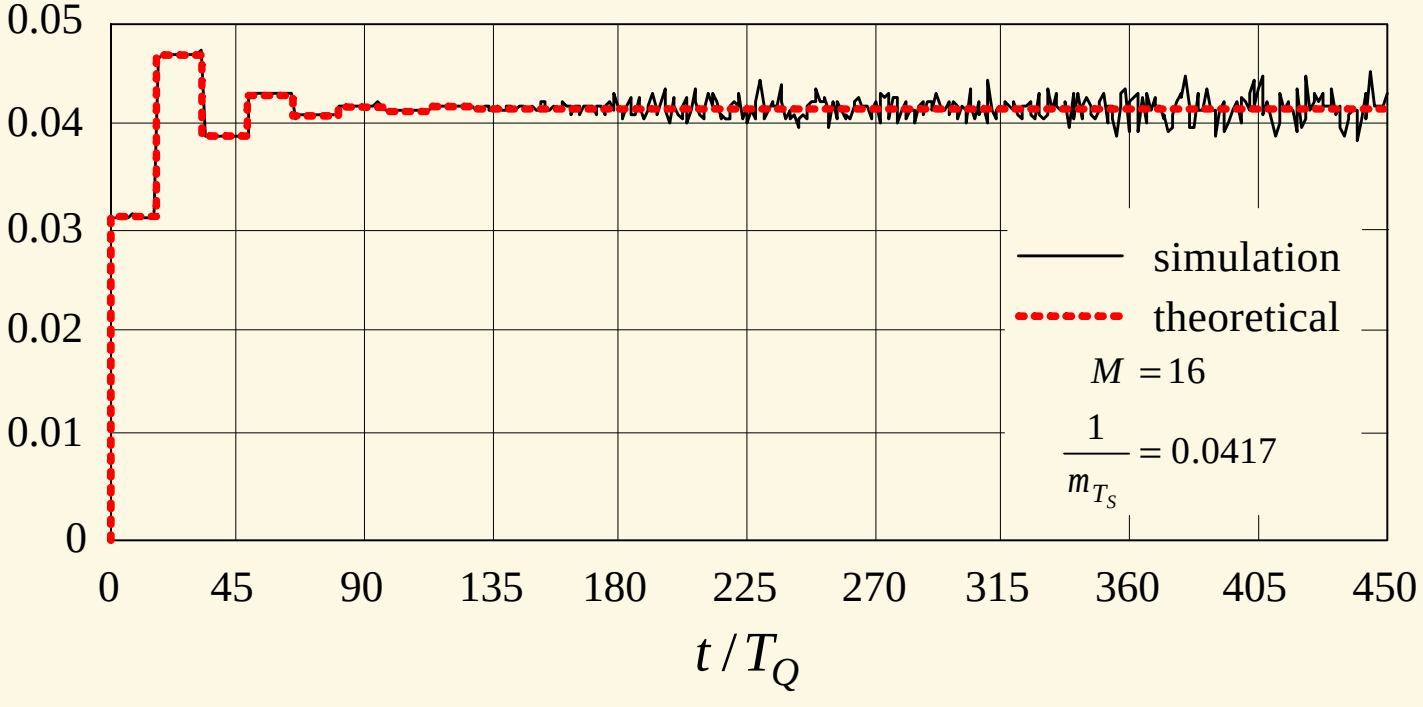
- Realize a constant sampling point density function (SPDF) ✓
- Avoid too short intersample times ✓



SD Design Requirements

2. Solution (optimized)

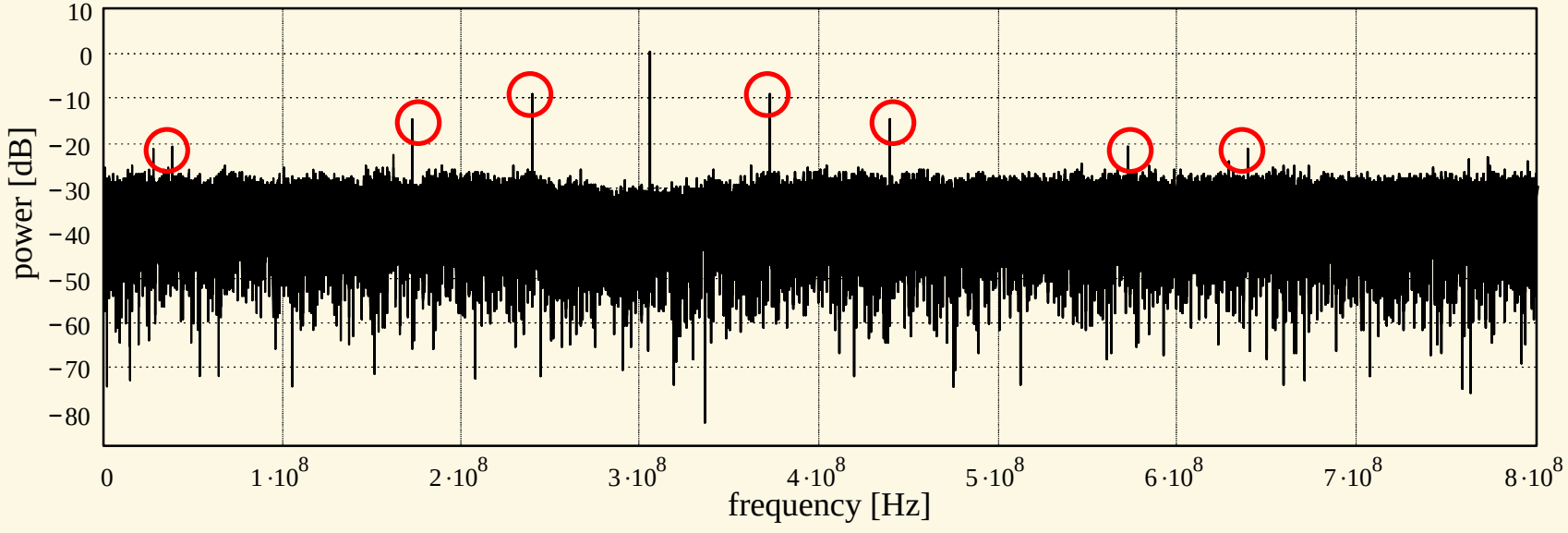
Sampling point density function (SPDF)
theoretical vs. simulated results



SD Design Requirements

- PDF of sampling instances **NOT MATCHED** to SD system clock period
  → spurious frequencies in signal spectrum

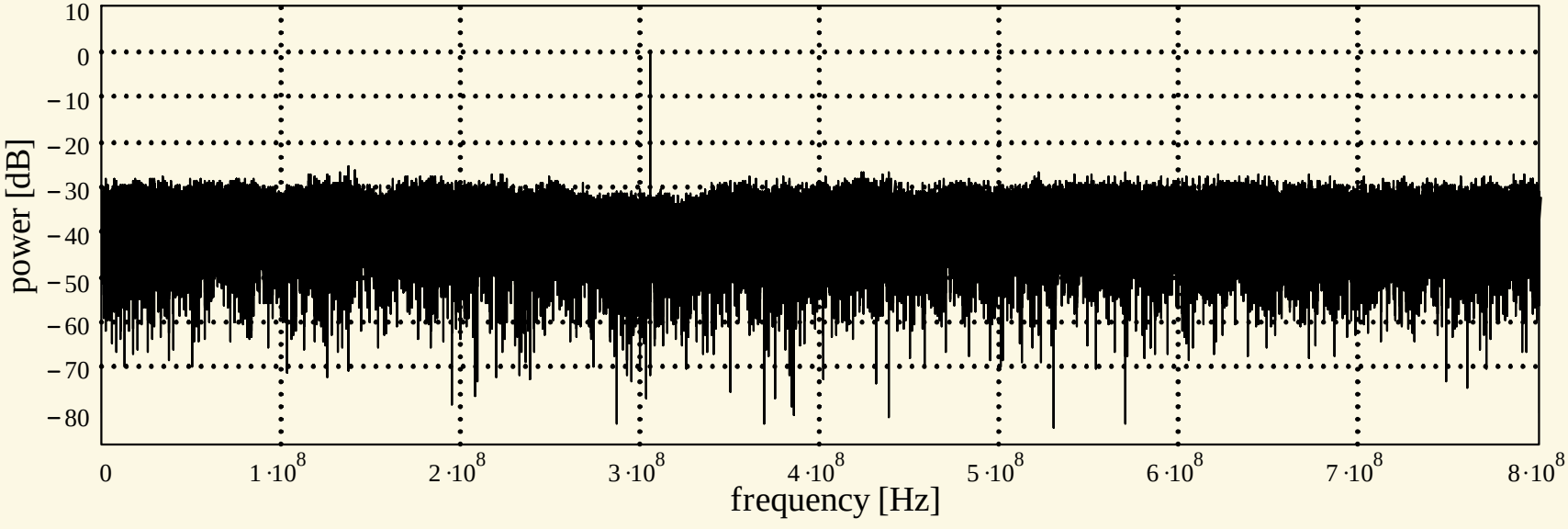
$$f_{signal} = 305MHz \qquad m_{T_S} = 15ns \qquad s_{T_S} = 4.1ns$$
$$T_{clk} = 15ns \qquad T_Q = 625ps \qquad \max\{e_k T_Q\} = 10ns$$



SD Design Requirements

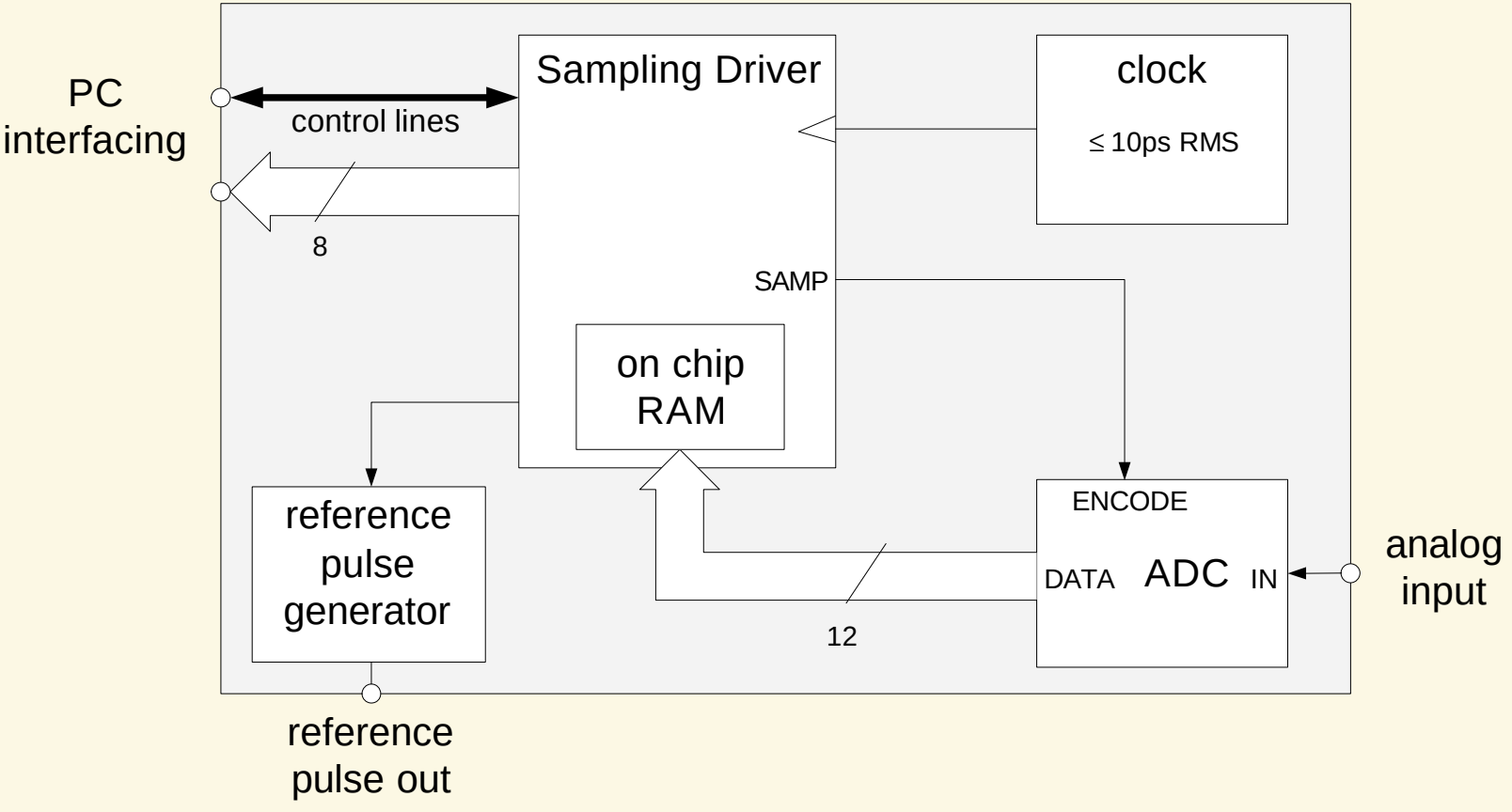
- PDF of sampling instances **MATCHED** to SD system clock period
  → spurious frequencies disappear

$$f_{signal} = 305MHz \qquad m_{T_S} = 10ns \qquad s_{T_S} = 4.1ns$$
$$T_{clk} = 10ns \qquad T_Q = 625\,ps \qquad \max\{e_k T_Q\} = 10ns$$



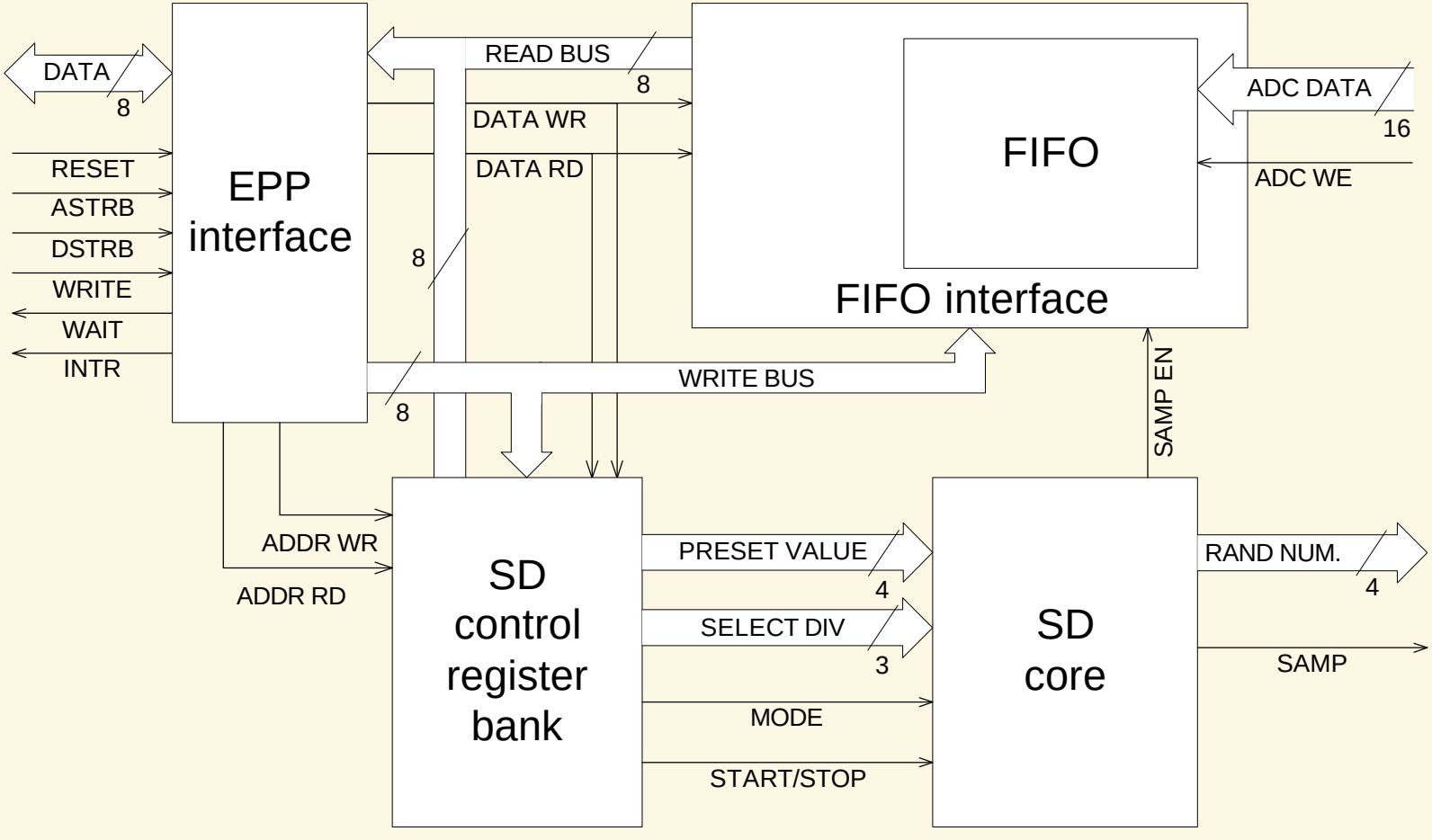
Architecture and Scalability

Non-uniform Sampling Device



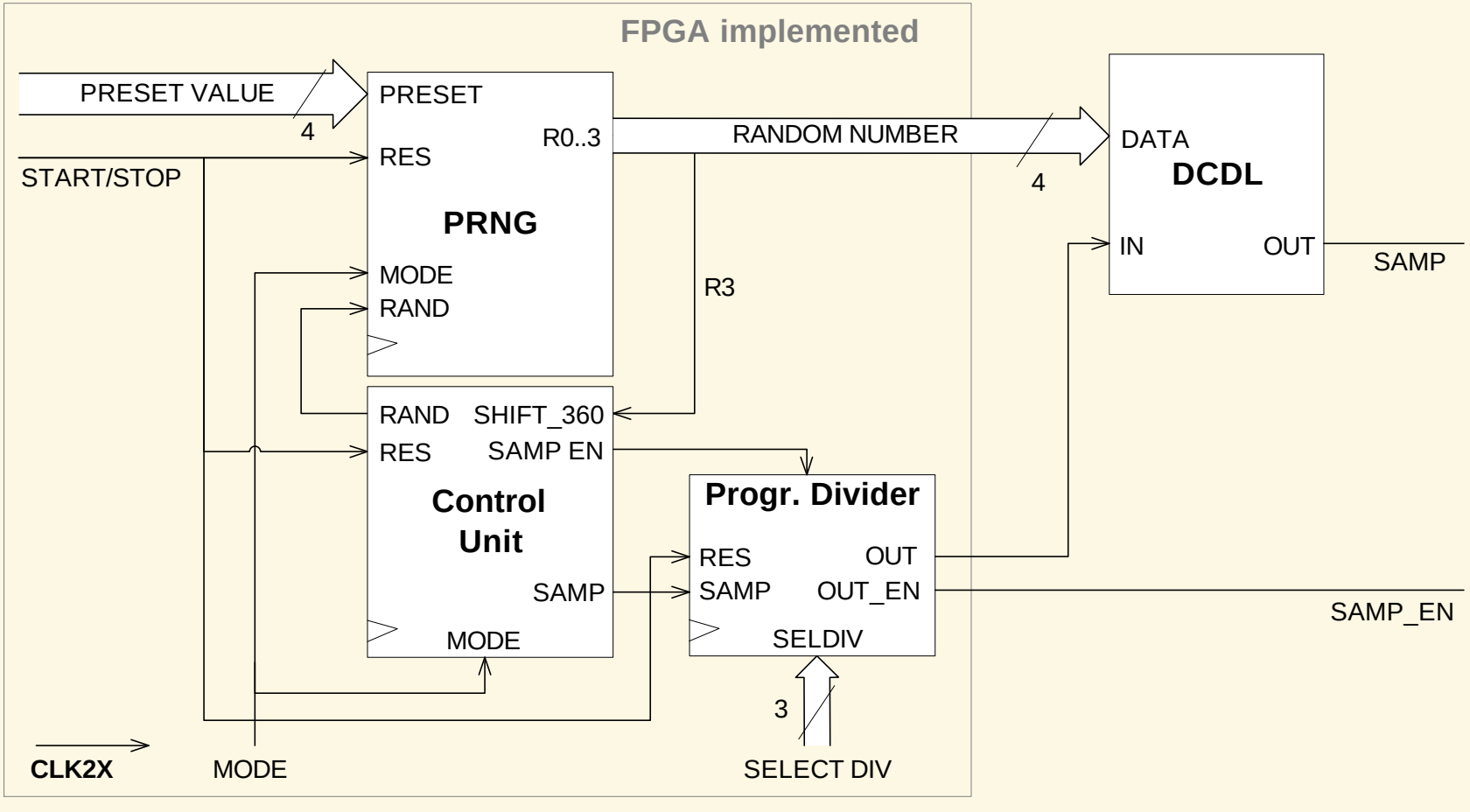
Architecture and Scalability

Sampling Driver Architecture (DCDL not included)



Architecture and Scalability

Sampling Driver Core



Architecture and Scalability

Summary

- Scalable SD parameters (VHDL generics)
  - FIFO depth and width (within FPGA limits)
  - PRNG length
  - Width of DCDL tap
- Currently realized design properties
  - Max. clock frequency 100MHz (200MHz internal - DLL)
  - FIFO size 12bit address width 16bit data width
  - Design fits into XILINX XCV300E (VIRTEX 300k system gates)
  - EPP interface to PC

Architecture and Scalability

Sampling Driver – VHDL Test Bench