Network-on-Chip Communication Grids for High Performance Packet Processing

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ABSTRACT

Since the demands on performance and flexibility for packet processing are rising permanently, FPGAs and ASICs are the preferred hardware platform due to their high computation power. But existing solutions for packet processing in FPGAs and ASICs base on conventional, synchronous bus systems or pipelined data path architectures, which are only little scalable and can not fulfill these requirements in the near and far future. Driven by the so called design-productivity-gap, new architectures for on-chip communication and information processing are needed, which can handle Gigabit data rates and beyond, allow for IP reuse, and reduce the systems complexity. In addition, current design flows can not effectively exploit the potential of the high number of processing elements and functional blocks that is available on a single integrated system today. The latest approaches are the Network-on-Chip paradigm and globally asynchronous and locally synchronous architectures. Although Networks-on-Chip are mostly used in ASIC designs, this contribution discusses the feasibility of Networks-on-Chip on FPGAs as communication grid for computation-intense applications in the light of Internet packet processing. An example, plain and straightforward implementation of a Network-on-Chip is presented, that omits sophisticated auxiliary features, e.g., for Quality-of-Service. A low-end Network-on-Chip leaves valuable logic resources of the FPGA for the functional part of a design. It is shown that a simple realization provides sufficient on-chip communication performance to handle highest data rates with modest effort. Furthermore, the realization of hardwired, embedded Networks-on-Chip in FPGAs is proposed.

Categories and Subject Descriptors

B.4.3 [**Input/Output and Data Communications**]: Interconnection (Subsystems) – *Asynchronous/synchronous Operation, Interfaces, Topology (e.g., bus, point-to-point)*

B.5.1 [**Register-Transfer-Level Implementation**]: Design – *Data-path Design, Design Styles*

C.2.0 [**Computer-Communication Networks**]: General – *Data communications, Open Systems Interconnection reference model (OSI)*

General Terms

Design, Performance

Keywords

Network-on-Chip, System-on-Chip, Packet Processing, GALS, FPGA, Simplicity