An Integrated Hardware Solution for Mac Address Translation, MPLS-UNI, and Traffic Management in Access Networks

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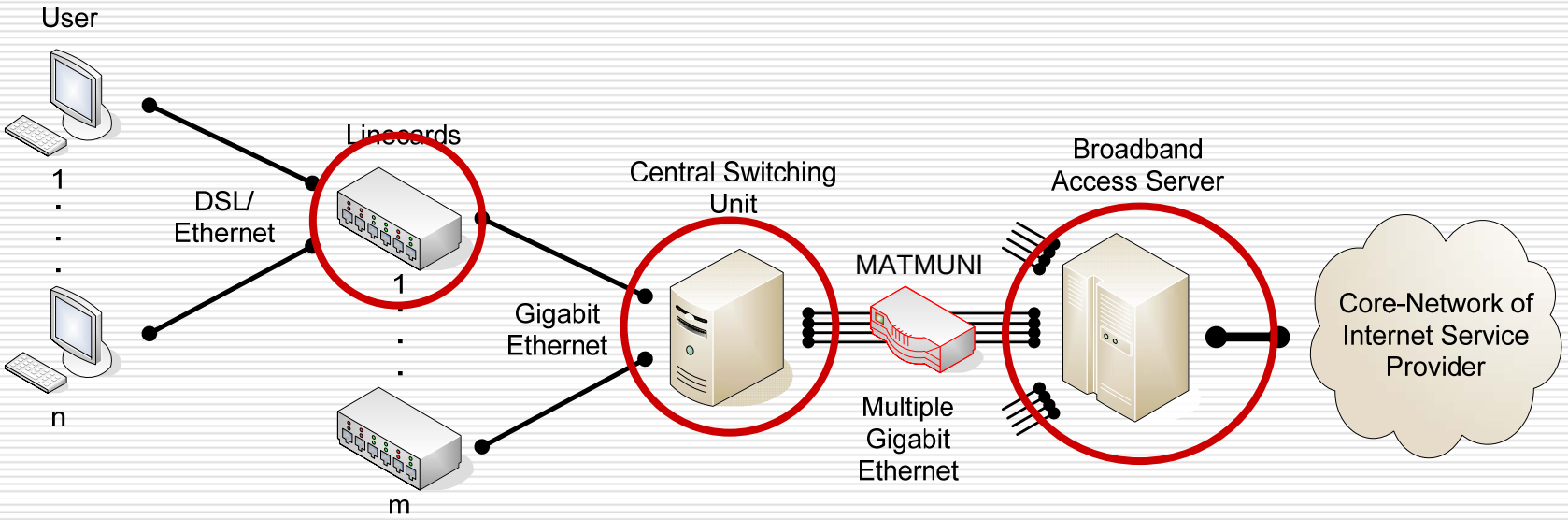
Outline

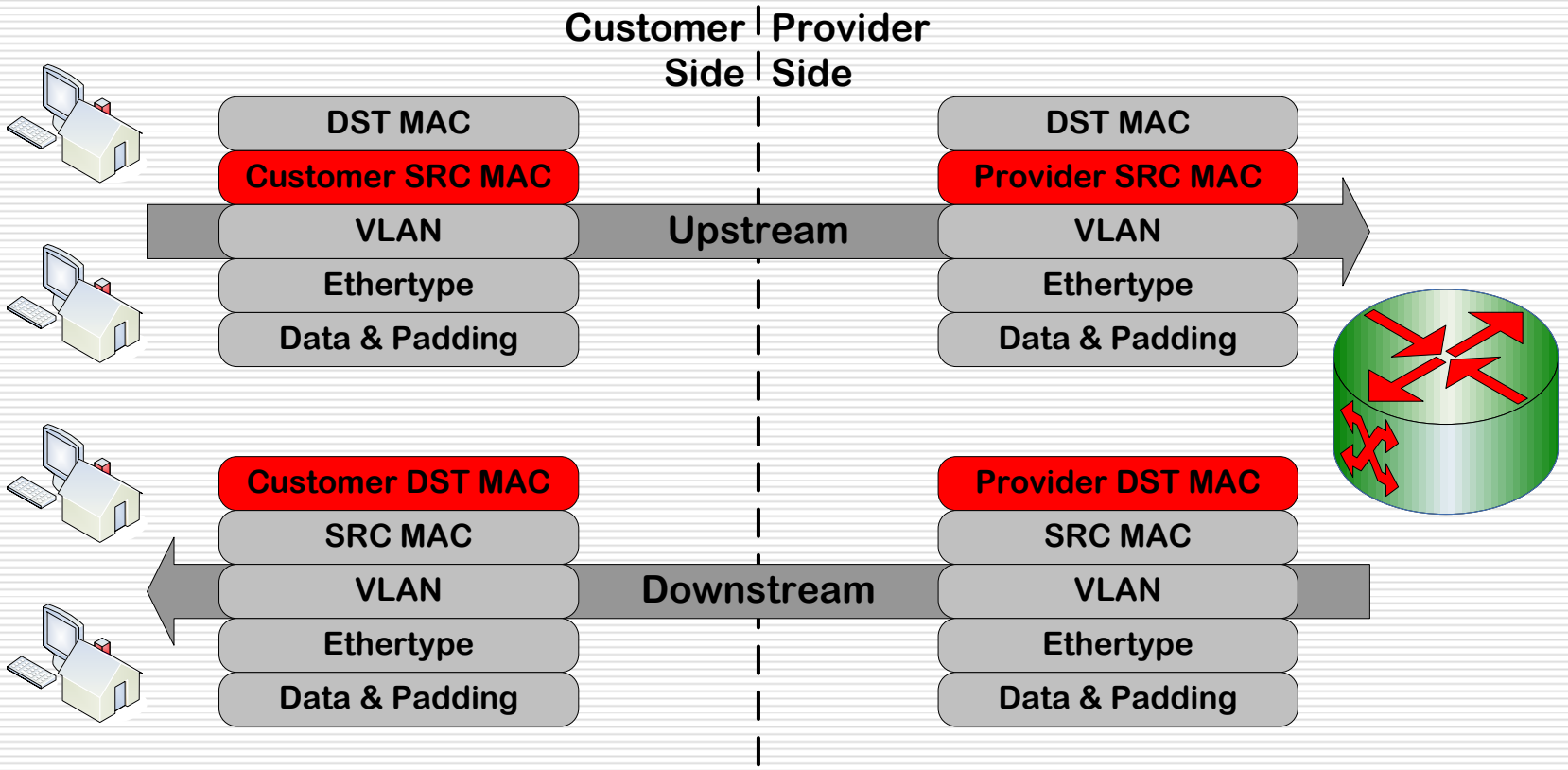
- Access Network Architecture
- MATMUNI – Functional Elements
  - The MAC Address Translation (MAT)
  - The Multi Protocol Label Switching-User Network Interface (MPLS-UNI)
  - The Traffic Management (TM)
- Architecture of FEs
- Functional Integration (MATMUNI)
- Conclusion

Access Network Environment



- Need for Differential Services, increased QoS
- MATMUNI as a combined solution targeting MAT, MPLS-UNI, and TM

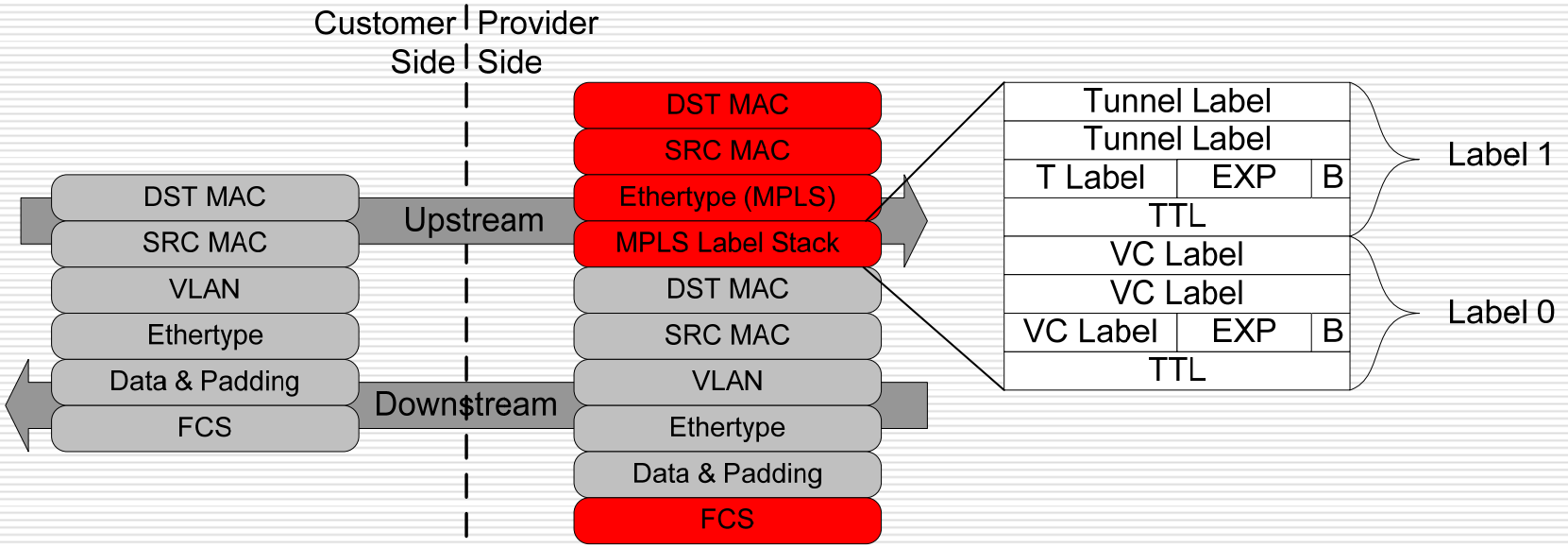
MAC Address Translation-MATMUNI



MAC Address Translation

- Scalability, flexibility
  - 1:1, n:1 and partial assignment of Provider-MAC
  - White list (just forward), black list (block)
- Protection against ARP spoofing
  - Attacks base on dynamic address table updates → but we have static address tables
  - DSL/Ethernet-flatrates are always on → „static“ address assignments
- Standards compliance
  - Frame size & header structure unchanged
  - Feasible with standard switching hardware

MPLS-Encapsulation

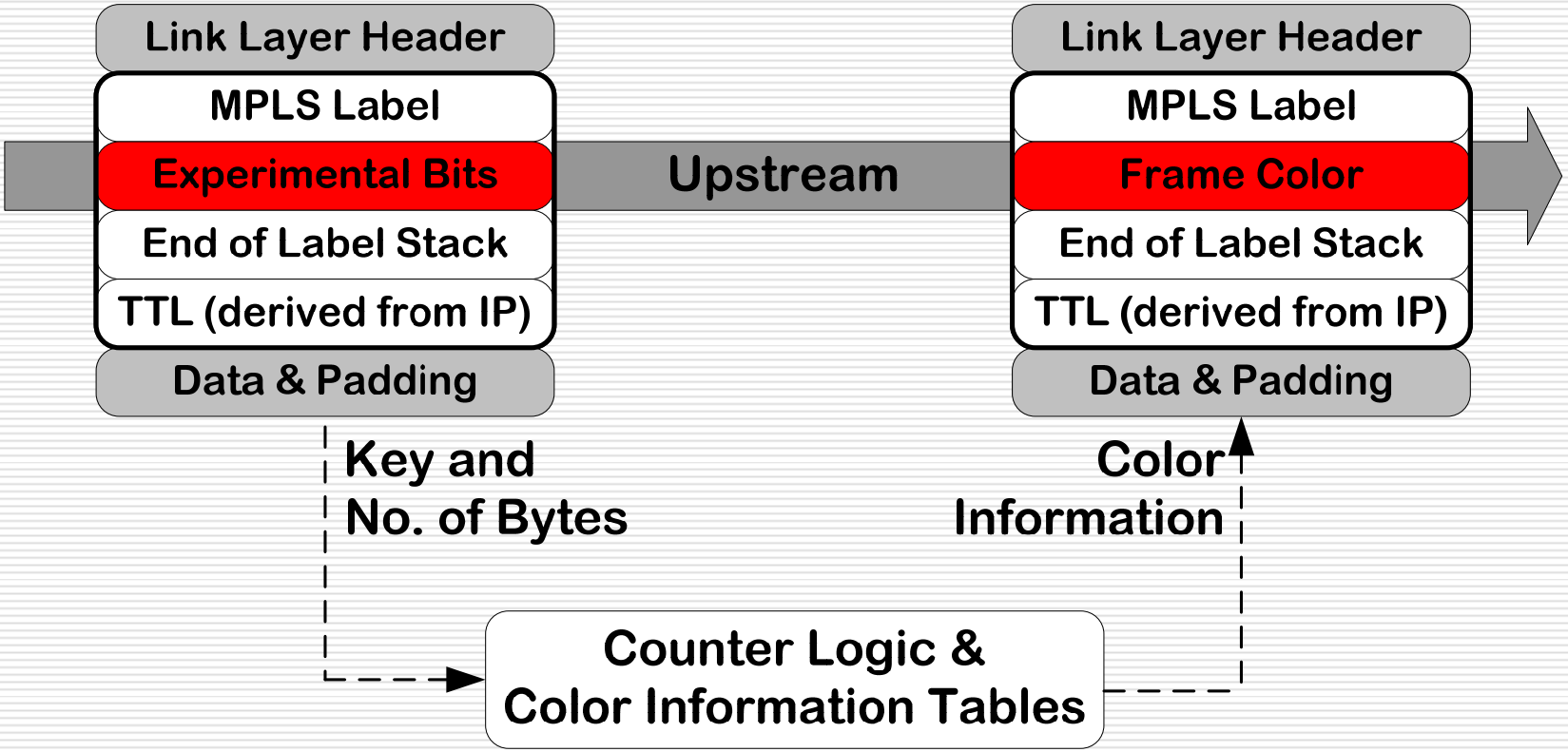


- MPLS Label Stack usually between layer 2 and layer 3 header
- We use encapsulation scheme by Martini

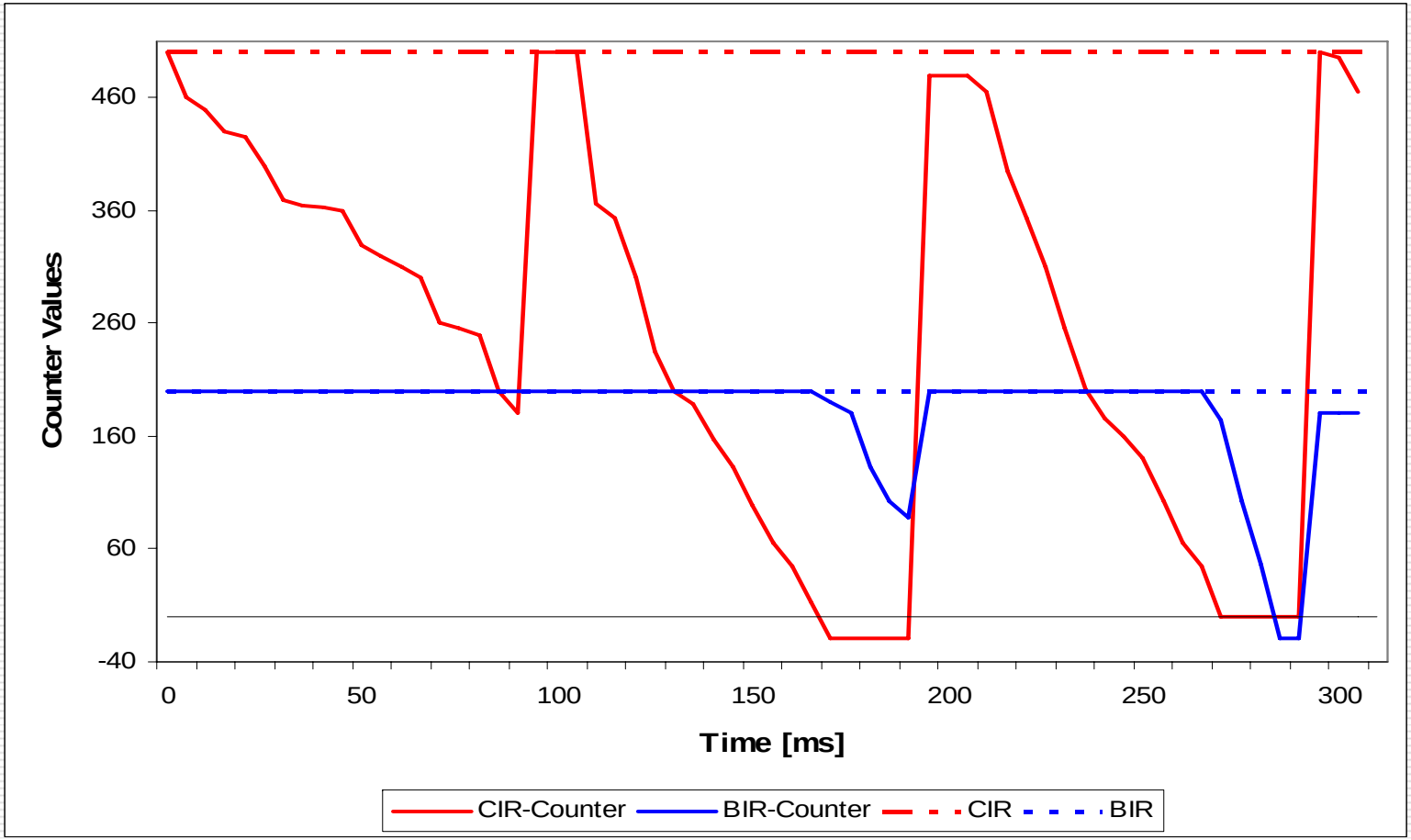
MPLS-User Network Interface (MPLS-UNI) - MATMUNI

- MPLS Label Stack container to carry information
- No complete LER implementation with an LDP running is necessary
  - Possibility to implement the whole system in Hardware
- Primary Functionality:
  - Upstream direction →insert an MPLS Label Stack
  - Downstream direction → remove MPLS Label Stacks

Traffic Manager - MATMUNI



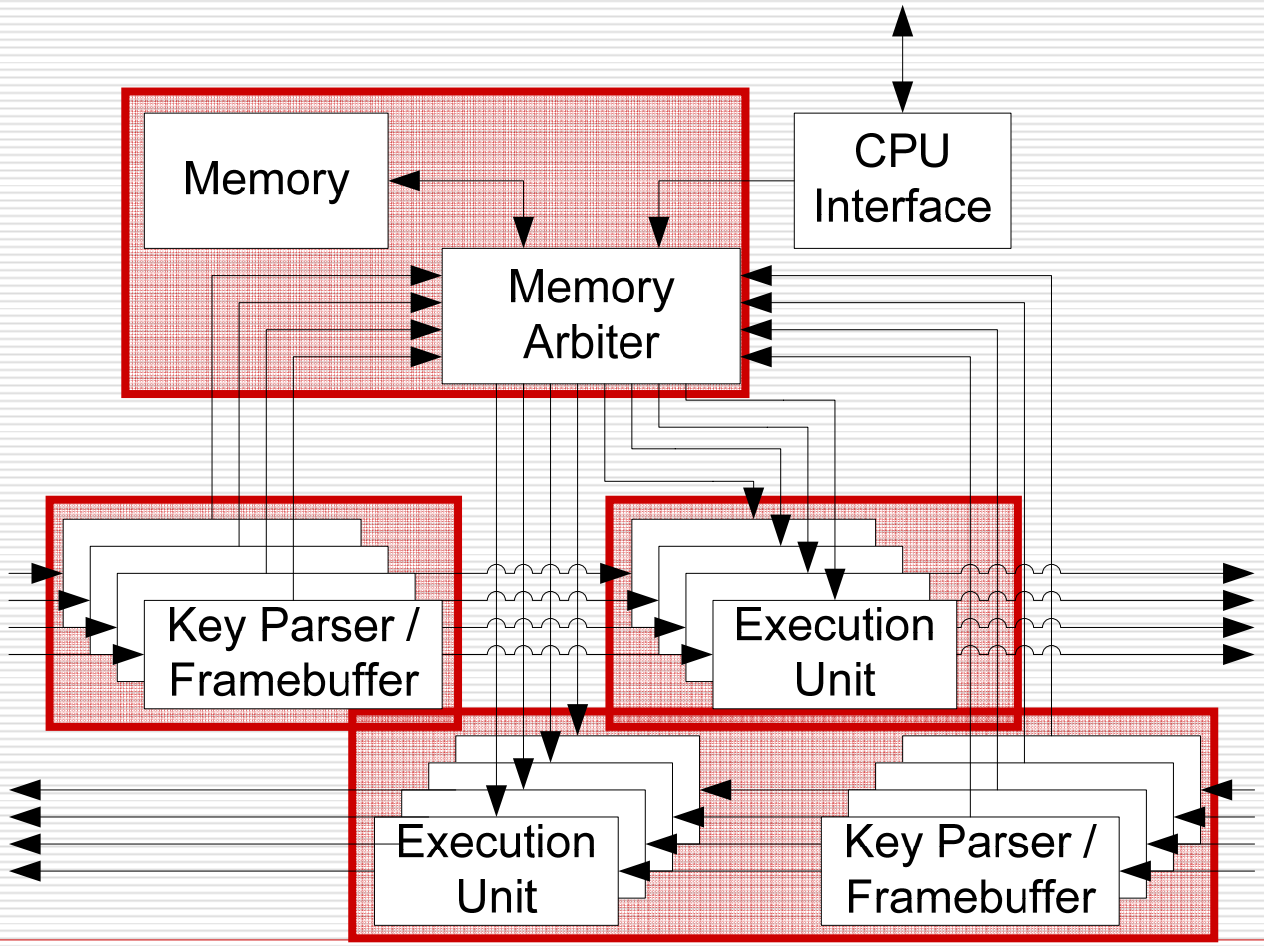
Traffic Manager



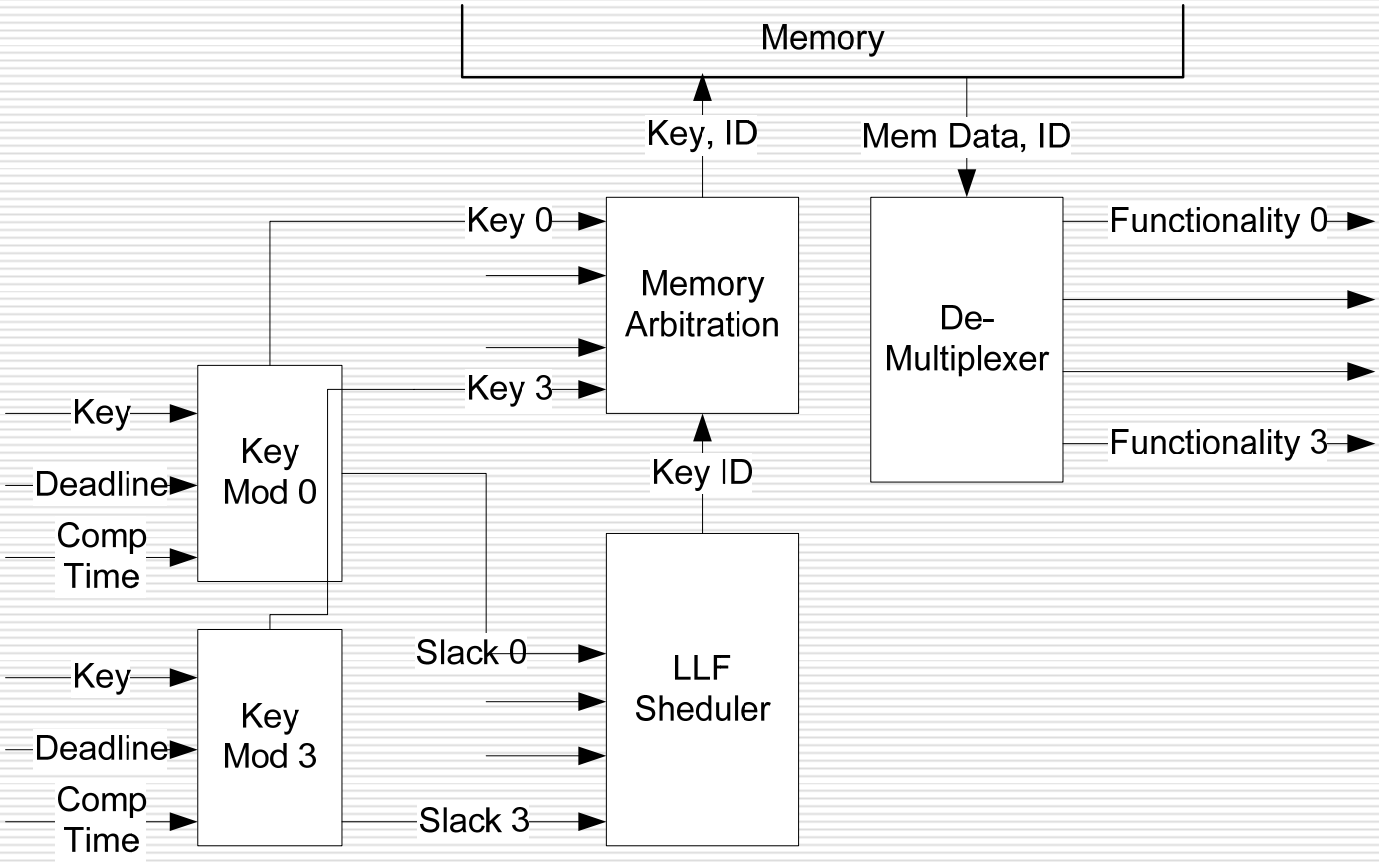
Traffic Manager

- Metering/congestion control already in access area
- Operates at wire speed
- Grants committed BW to customers in over-subscribed networks
- Fair
- Performs policing tasks by discarding red frames

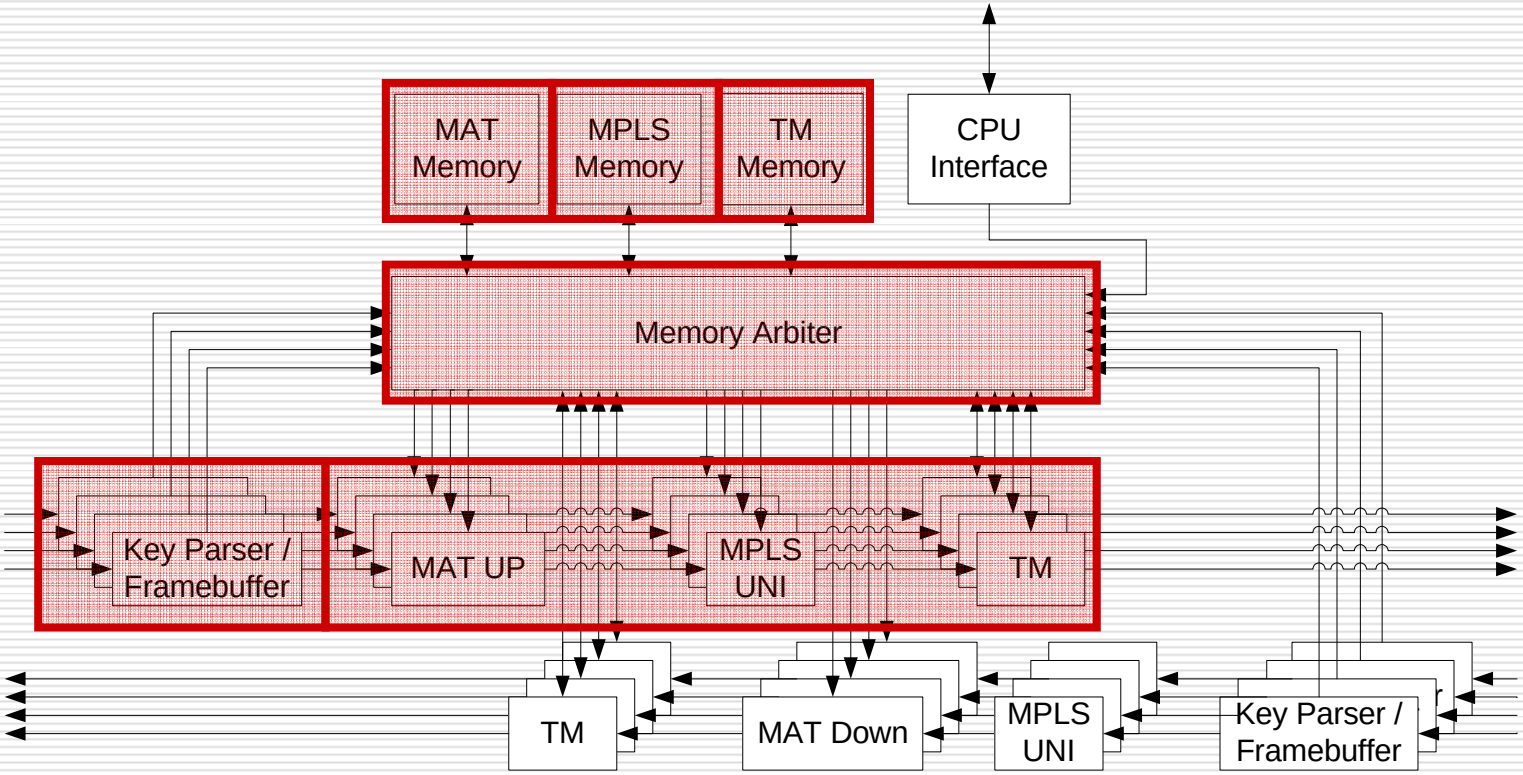
Module Architecture – Single Module



Memory Arbitration



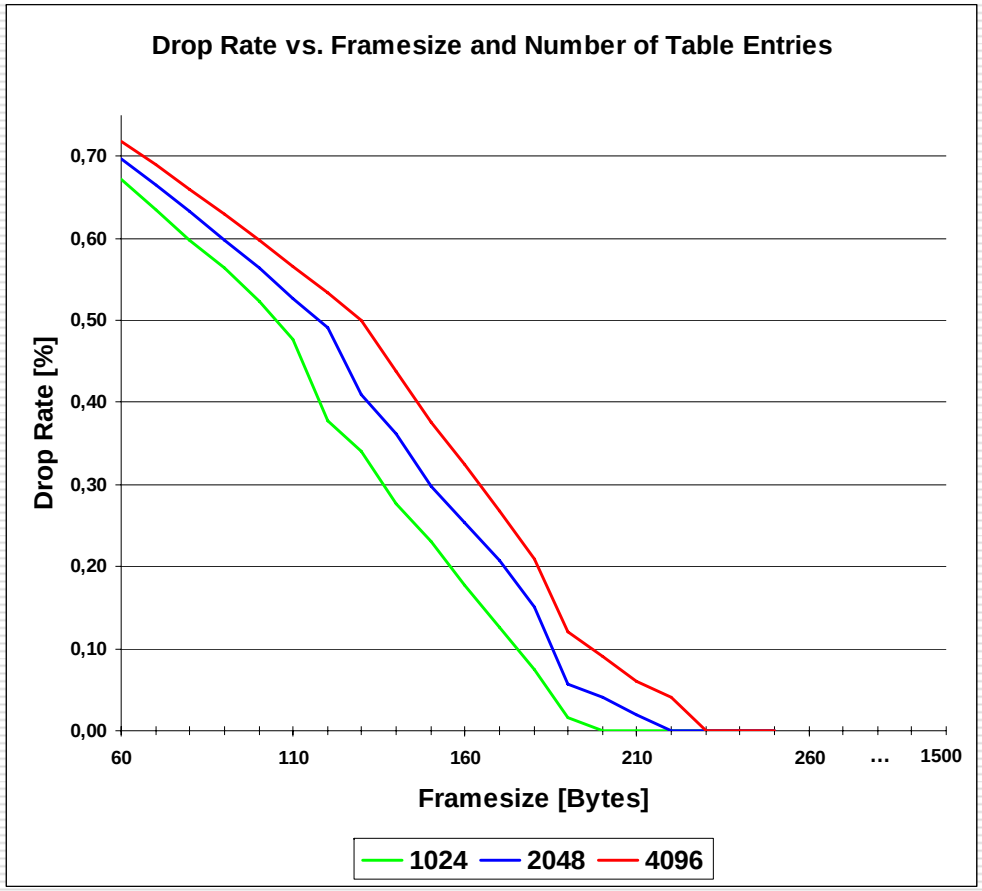
Architecture MATMUNI



Implementation Results (Xilinx Virtex 4 FX20-11)

Hardware Module	Speed in MHz	Area min/max
MATMUNI	140	2300/4300
MAT (UP & Downstram)	220	2x210
TM (UP & Downstream)	190	2x240
MPLS-Labeler	180	129
MPLS-Delabeler	320	101
Memory Arbiter	160	282/1023
CPU Arbiter	160	640
Key Parser & Framebuffer	150	336/723
Framebuffer	180	205

Simulation Results



- 8 independent GbE channels
- Artificial traffic
  - only minimal frames
- Realistic traffic
  - 35 % minimal
  - 11 % average
  - 10 % maximal
  - 44 % random
  - → no packet losses
- Average latency 130 cycles (≈1 us for GbE)

Conclusion

- Powerful and cost-effective solution to integrate different Functionalities into the Access Network area
- @125 MHz, 4 Gbps can be handled
- Size of the system can be minimized considering the actual tasks
- Functional spectrum can be broadened, due to reconfigurable HW