Deep Submicron Technology: Opportunity or Dead End for Dynamic Circuit Techniques

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Outline

- Introduction
  - Fundamentals
  - Technology development
  - Motivation
- Actual work
  - Dynamic logic styles
  - Implementation
  - Results
- Conclusions & Outlook

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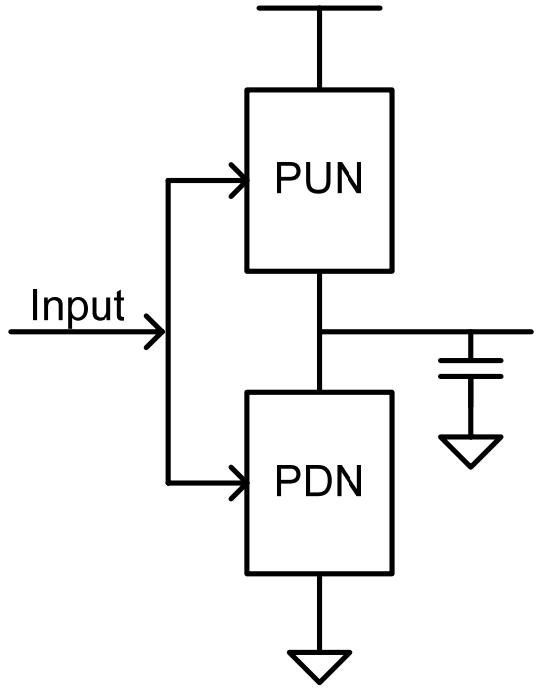
Fundamentals

Static CMOS

- Reliable
- Scalable
- Automated design tools available
- Good compromise of speed, size, power consumption



Static CMOS is and has been the dominating circuit technique

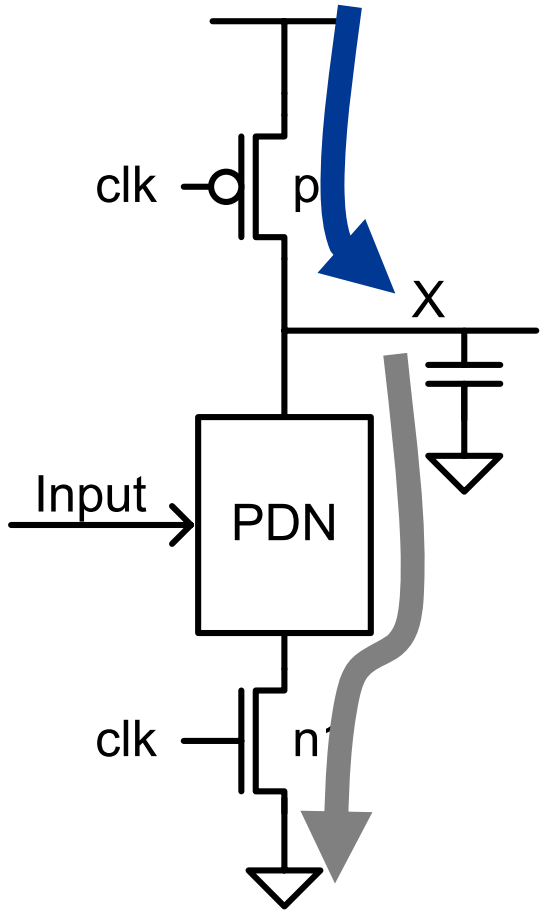
Fundamentals

Dynamic logic

Phases of operation:

- Precharge
  - clk = 0
  - X → 1
- Evaluation
  - clk = 1
  - X → 0
  - X = 1

} Depending on the input



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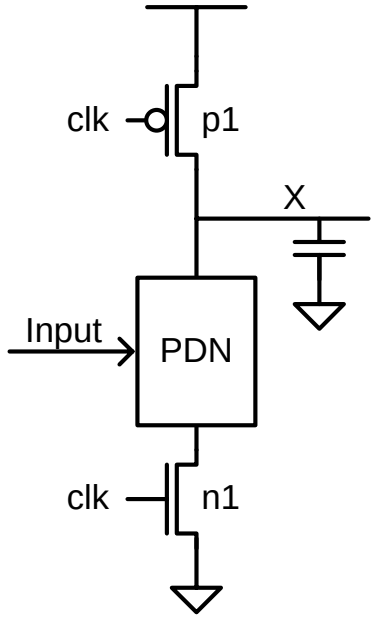
Fundamentals

Dynamic logic

- Fast
- Power hungry
- Susceptible to noise
- Difficult to implement



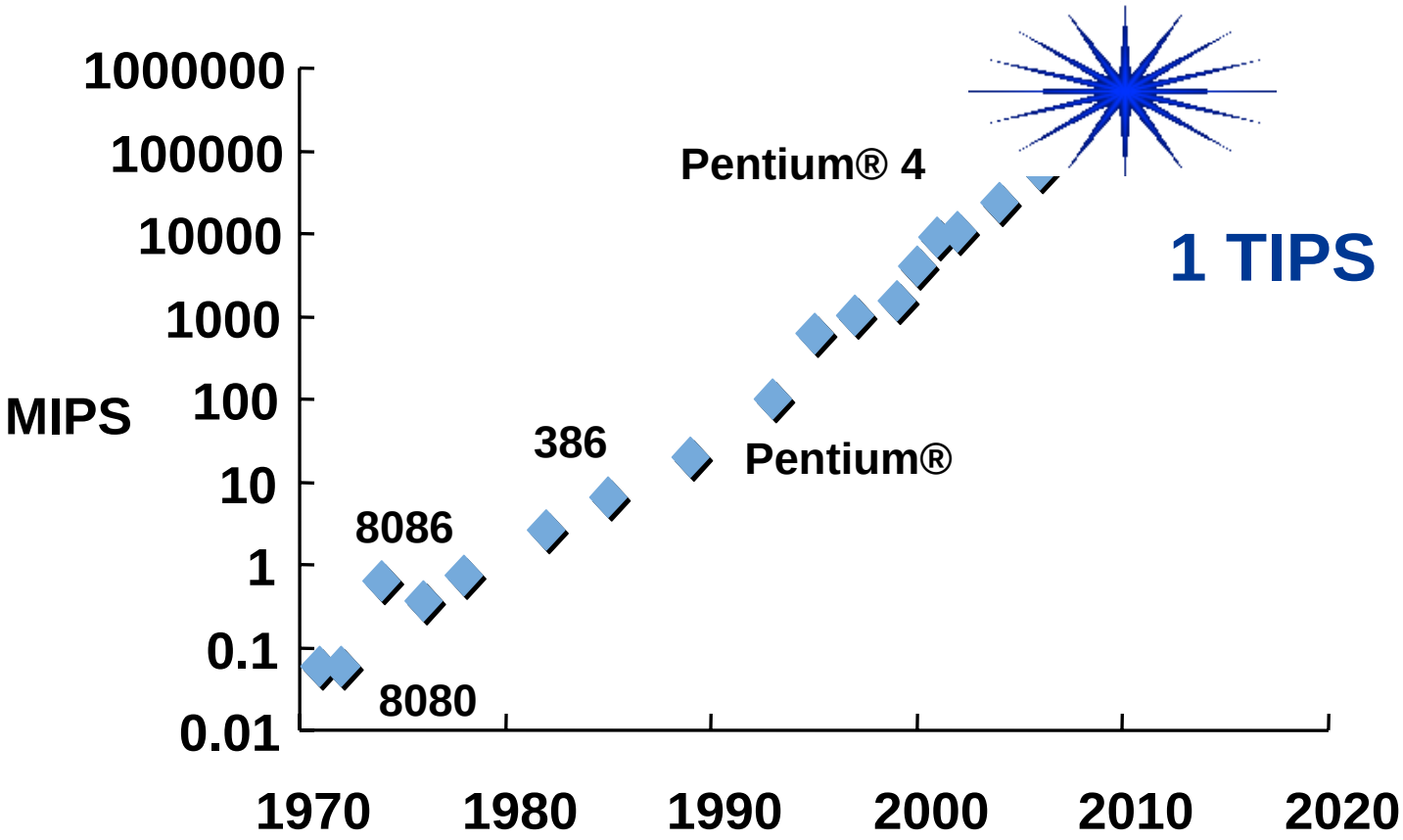
Continuously used to boost performance

E.g.	Intel Pentium 4	[Deleganes, 2004]
	IBM Power4	[Warnock, 2002]
	Sun Sparc V9	[Heald, 2000]

That is past and present, how about the future ?

Technology development

Performance



[Sery, 2002]

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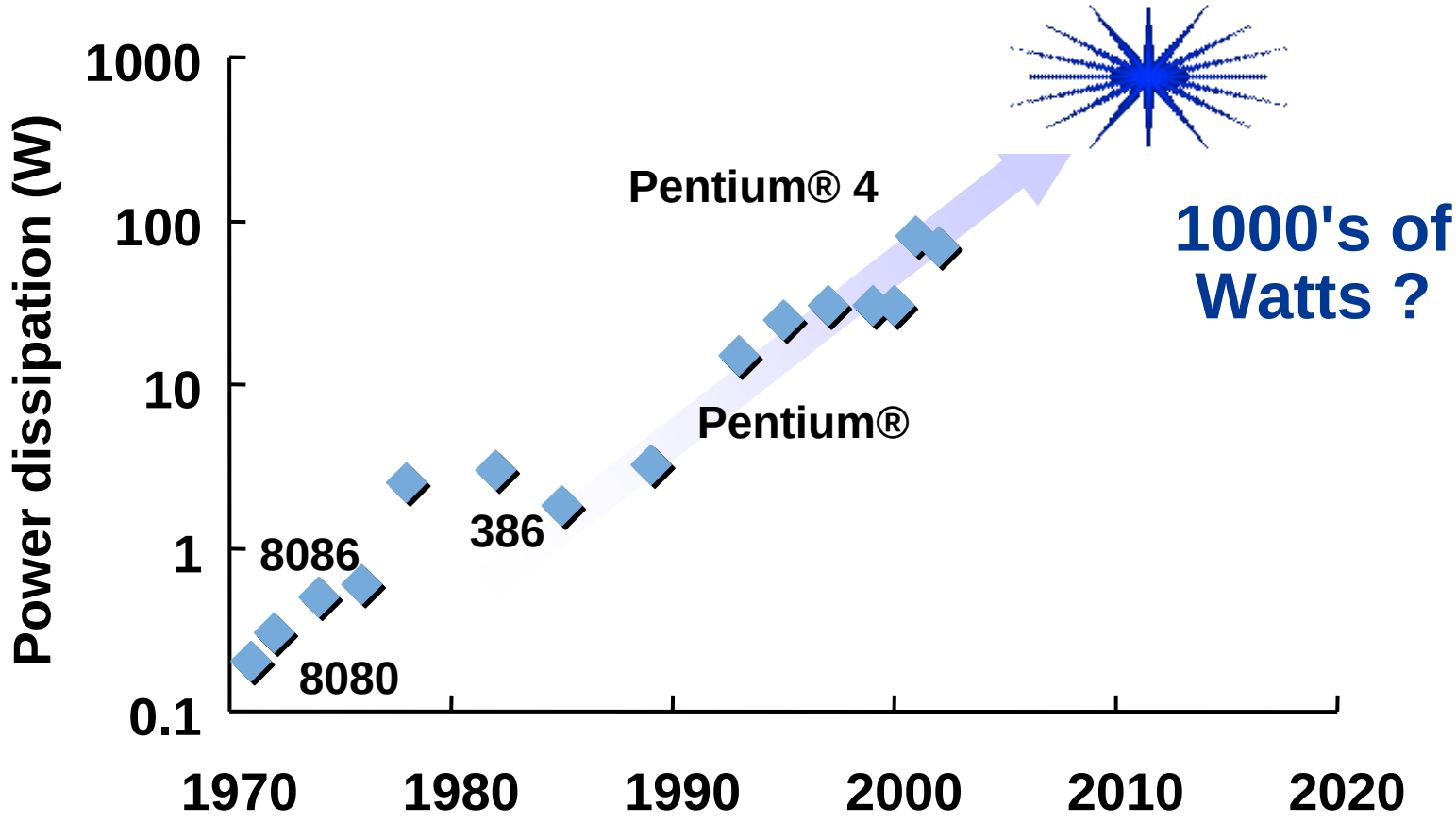
Technology development

Power dissipation



[Sery, 2002]

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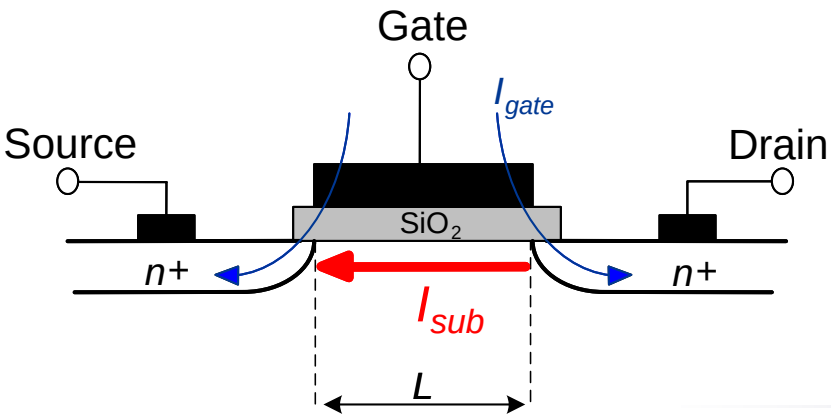
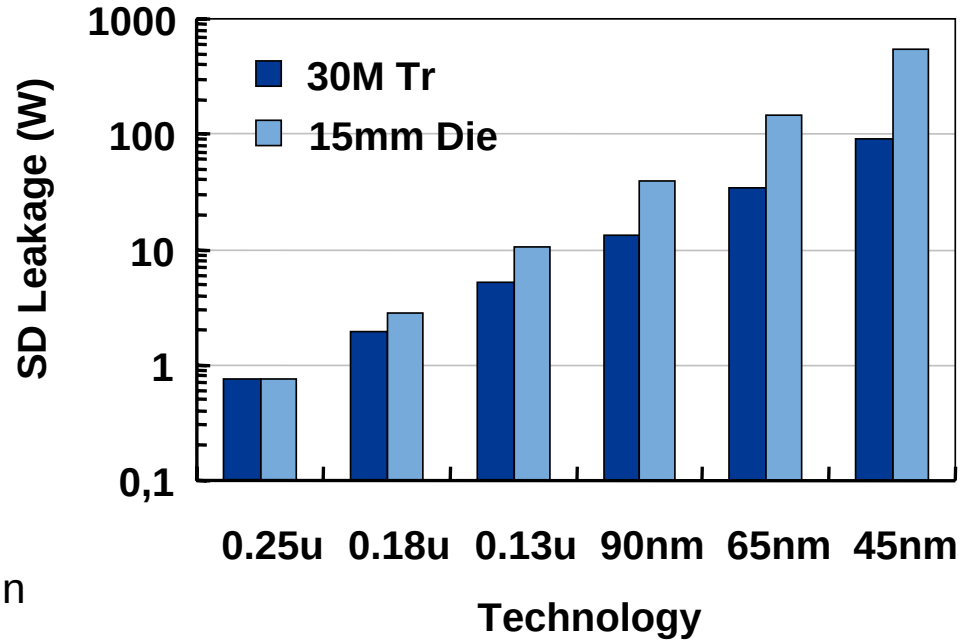
Technology development

Leakage currents

- Sub-threshold currents
- Reverse-biased currents
- Drain-Induced Barrier Lowering
- Gate-Induced Drain Leakage
- Punch-through Effect
- Narrow-Width Effect
- Gate-Oxide Tunneling
- Hot-Carrier Injection



[Sery, 2002]



Technology development

Interconnects

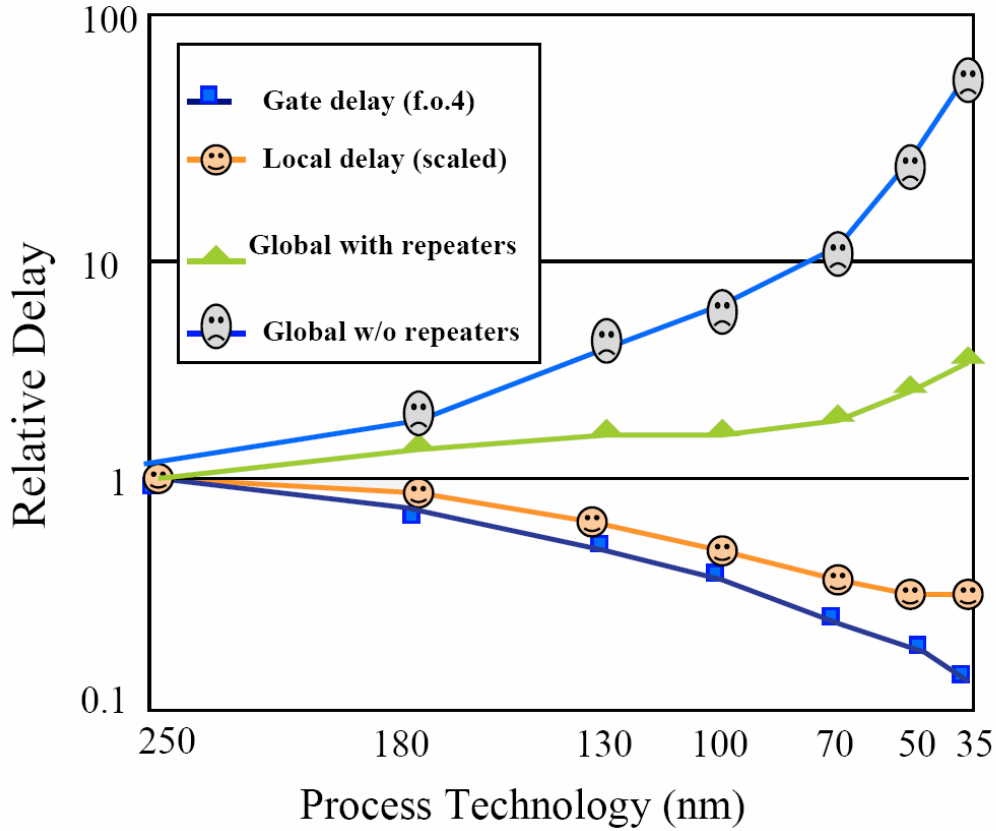
Propagation delays of global wires will be a multiple of the clock cycle.

Example (very optimistic):

6–10 clock cycles in 50nm technology

[Benini, 2002]

[Tenhunen, 2005]



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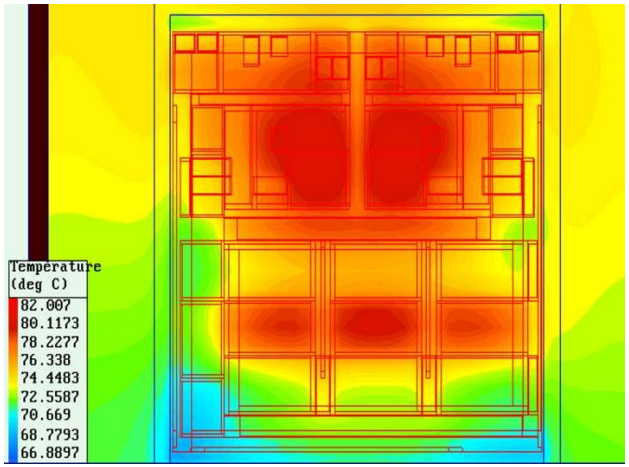
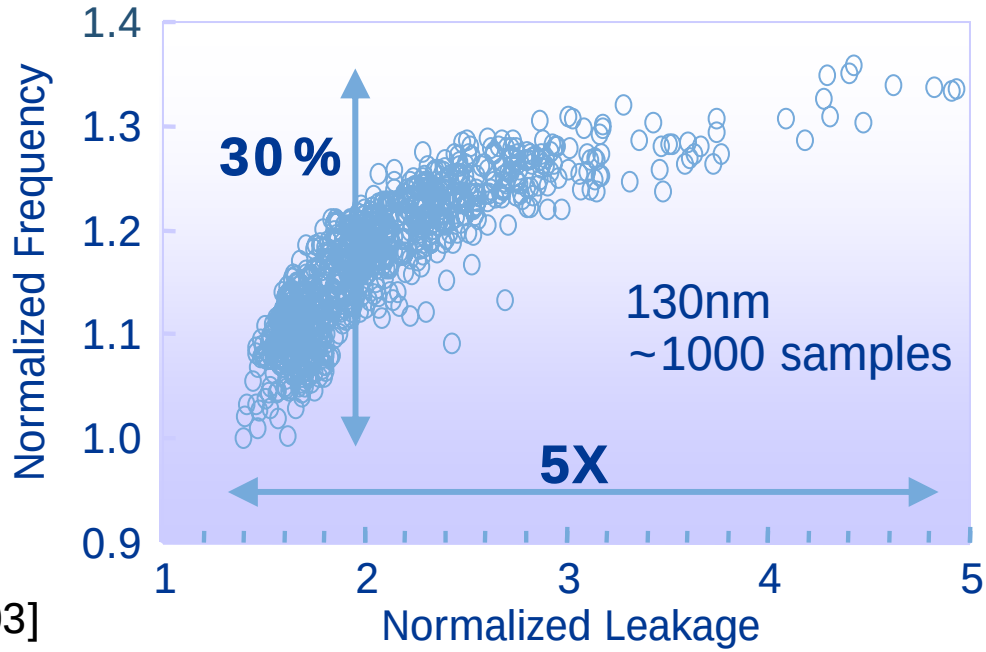
Technology development

Parameter variability



Power4 Server Chip

[Devgan, 2003]



[Borkar, 2005]

L (nm)	250	180	130	90	65	45
Vt (mV)	450	400	330	300	280	200
σ-Vt (mV)	21	23	27	28	30	32
σ-Vt/Vt	4.7%	5.8%	8.2%	9.3%	10.7%	16%

[ITRS, 2003]

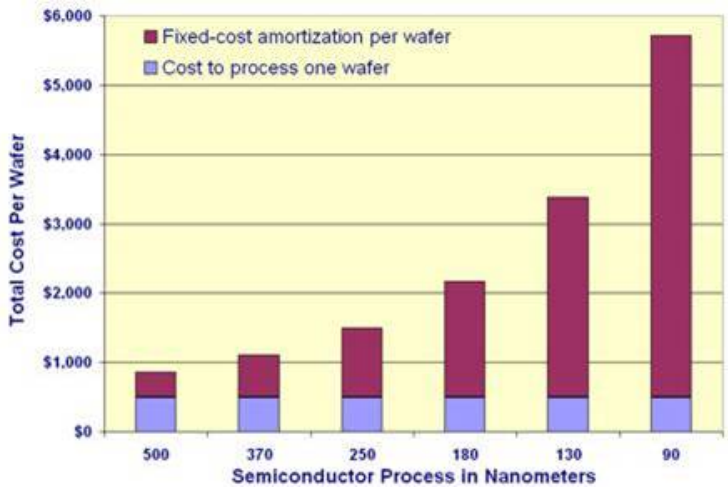
Parameter variability dramatically increasing

Technology development

Costs

Fixed costs per wafer are growing exponentially.

[Tredennick, 2003]



- Only high volume chips reasonable
- Number of ASIC design starts declining

Year	3 year design staff	Staff cost ($150k/Staffyear)
1997	210	90 M
1999	360	160 M
2002	800	360 M

Motivation

Consequence of the problems:

„Power outperforms Performance.”

Growth rate when new technology is introduced:

	Chip-Area	Power consumption	Performance
General Purpose Processors (GPP)	2X	2-3X	~1.4X

Requirements:

- More MIPS/mm²
- More MIPS/Watt

Motivation

- Large number of challenges
  - Well-known, but intensified issues
  - New issues
- Examination and determination of
  - performance parameters
  - associated limitations/conditions
  - possible applications

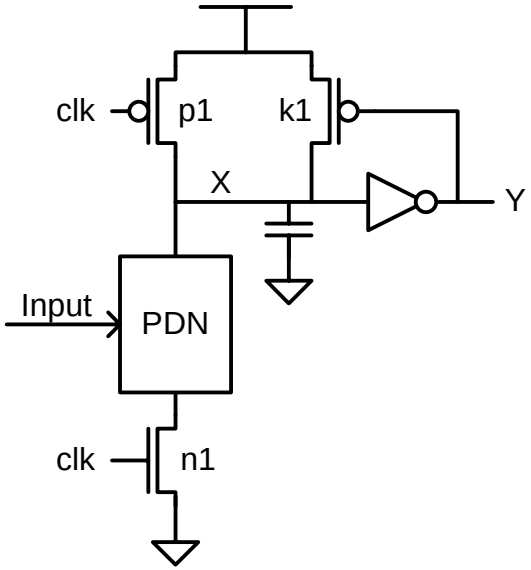
Deep Submicron Technology: **Opportunity** or **Dead End** for Dynamic Circuit Techniques?

Motivation

Related work

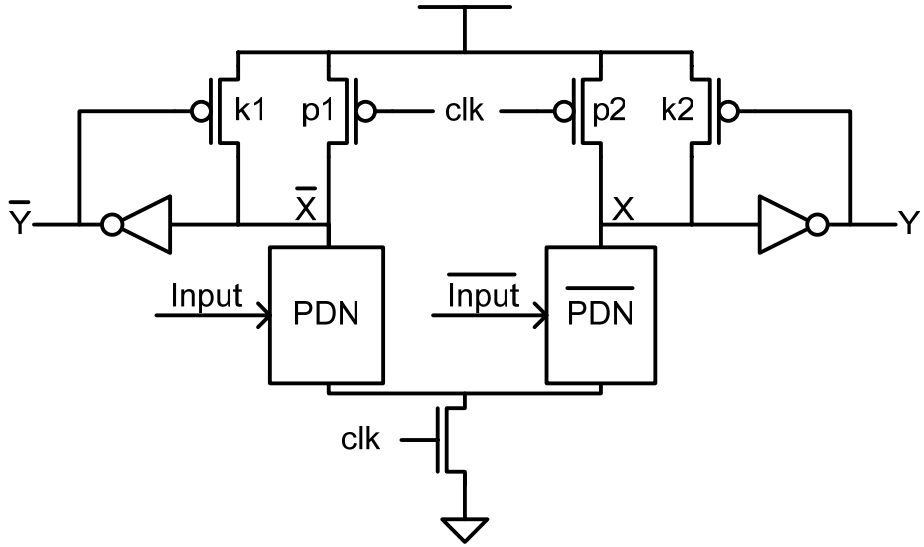
- Comparison of circuit techniques:
  - [Chu, 1987]
  - [Ng, 1996]
  - ...
- Domino logic won‘t work past 70 nm
  - [Anders, 2001]
- Demonstration of modified Domino in 45 nm
  - [Yang, 2004]

Dynamic logic styles



Single-rail Domino

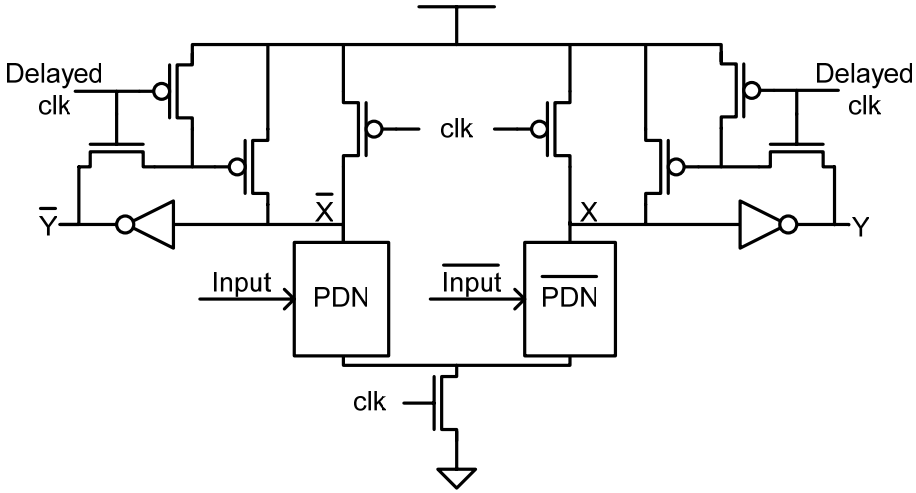
[Krambeck, 1982]



DCVS-Domino
(Differential Cascode Voltage Switch)

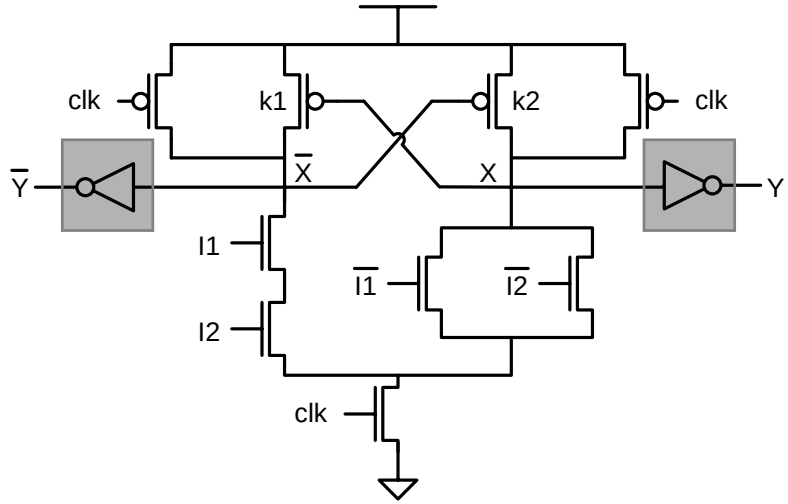
[Heller, 1984]

Dynamic logic styles



High-Speed Domino

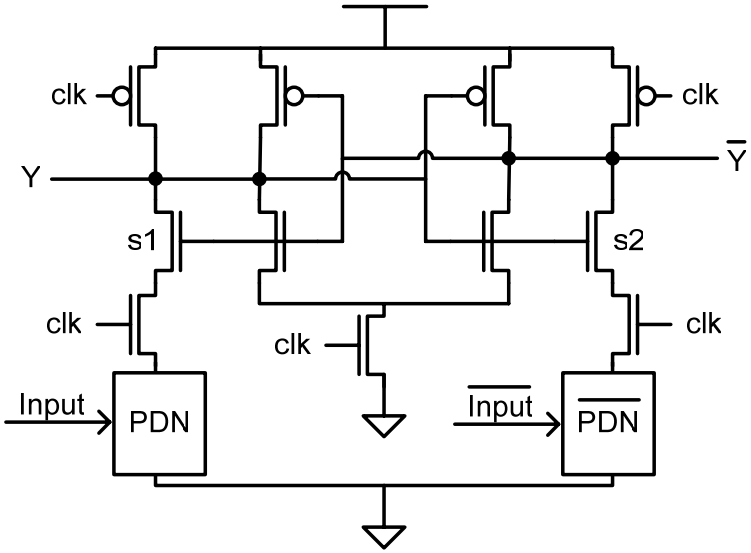
[Allam, 2000]



XC-Domino / XC-Differential
(Cross Coupled)

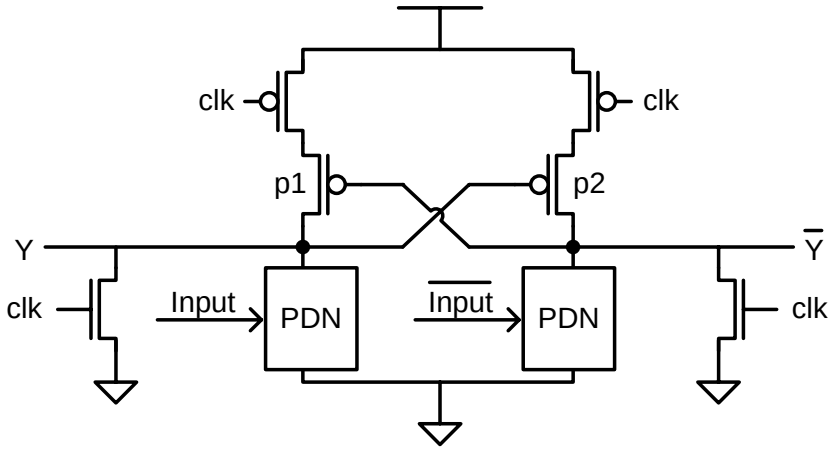
[Ng, 1996]

Dynamic logic styles



DCSL
(Differential Current Switch Logic)

[Somasekhar, 1996]



SPSD
(Sympathetic Precharged Static Domino)

[Gayles, 1997]

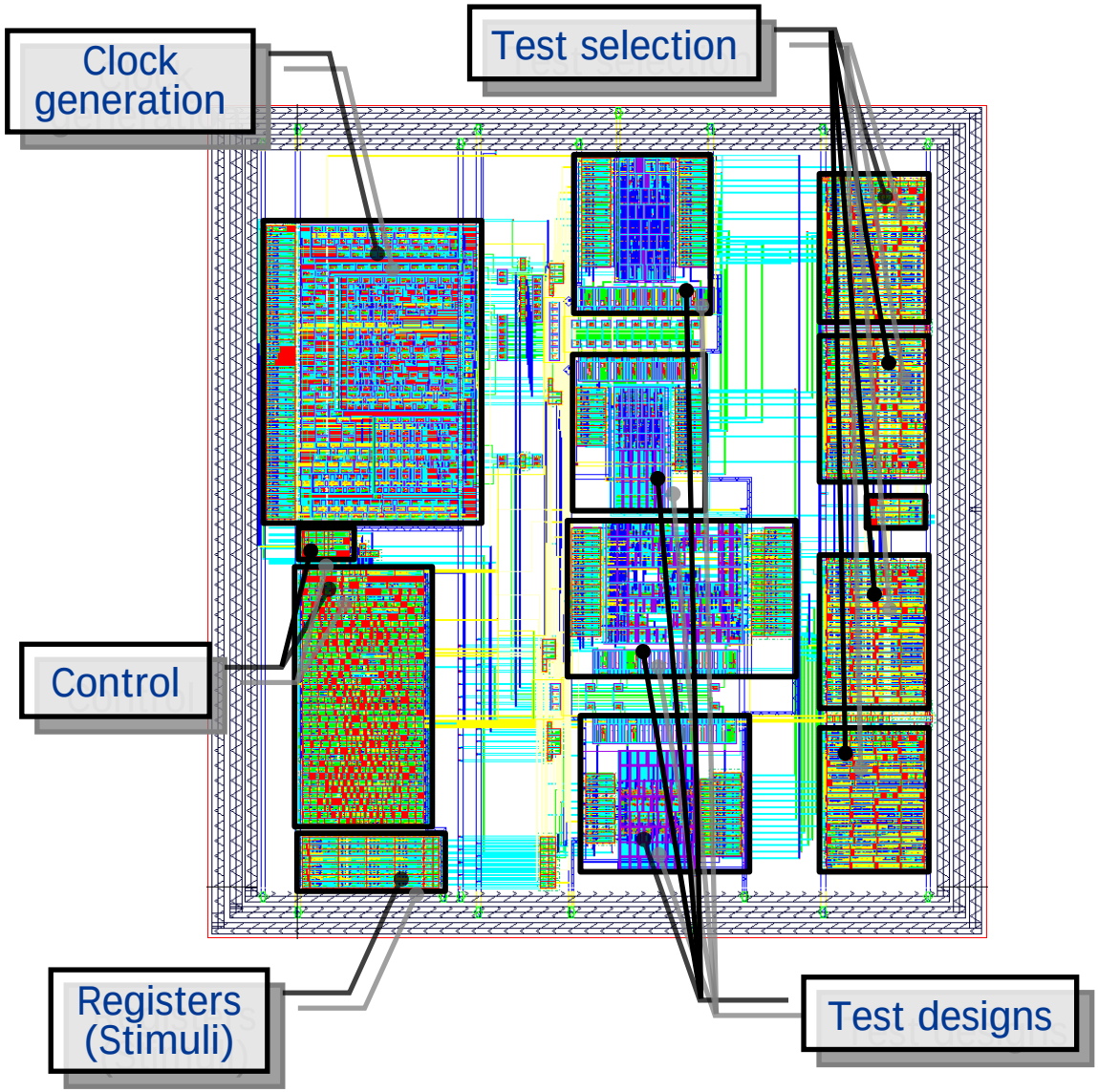
Implementation

Test designs

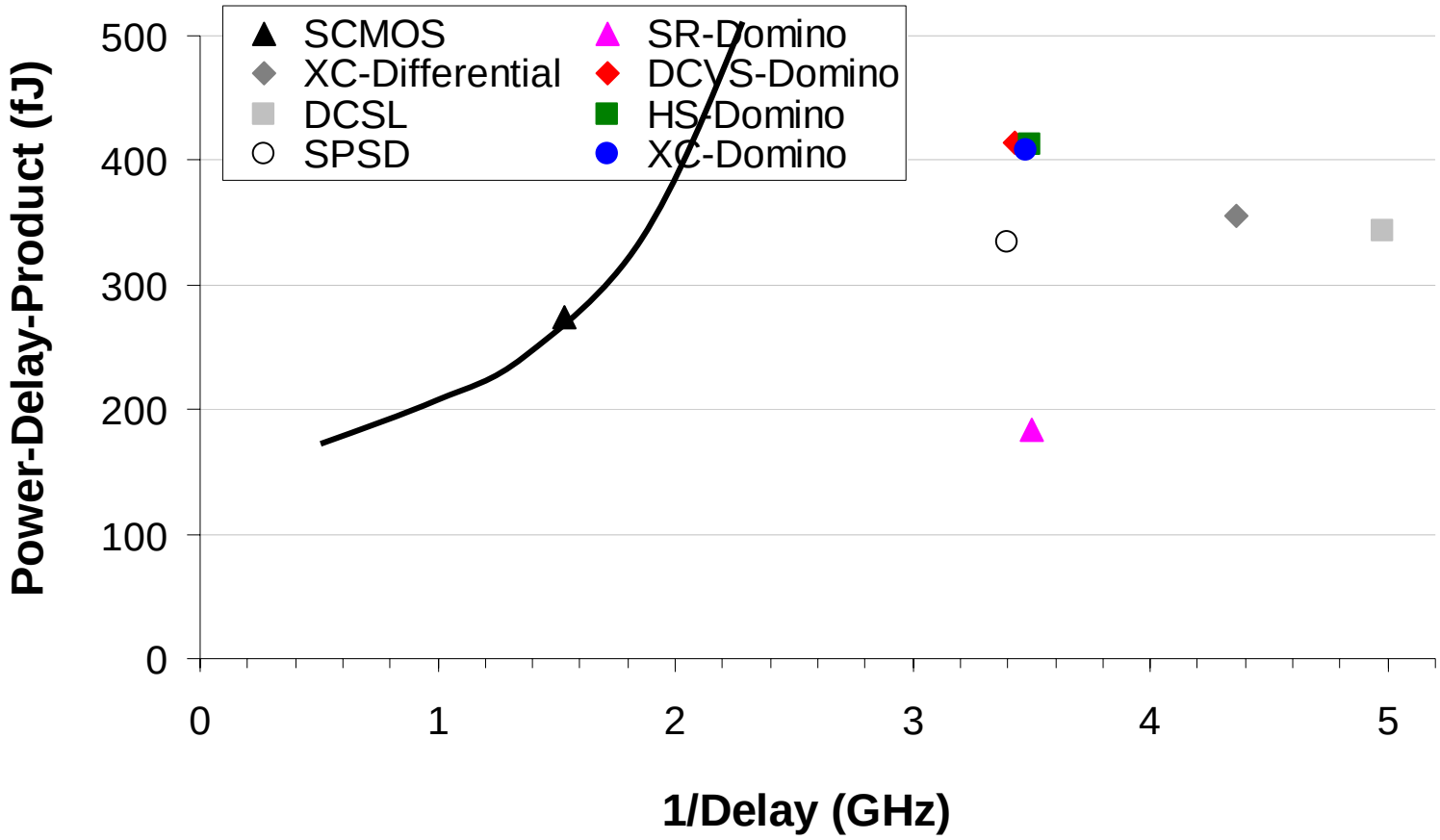
- Worst-case scenario
- Wallace multiplier
- Several logic specific
- Influence of sizing

Test chip

- Prototype (90 nm)
- Modular
- 64 designs for test
- Measurement of
  - Functionality
  - Delay
  - Frequency
  - Power



Results



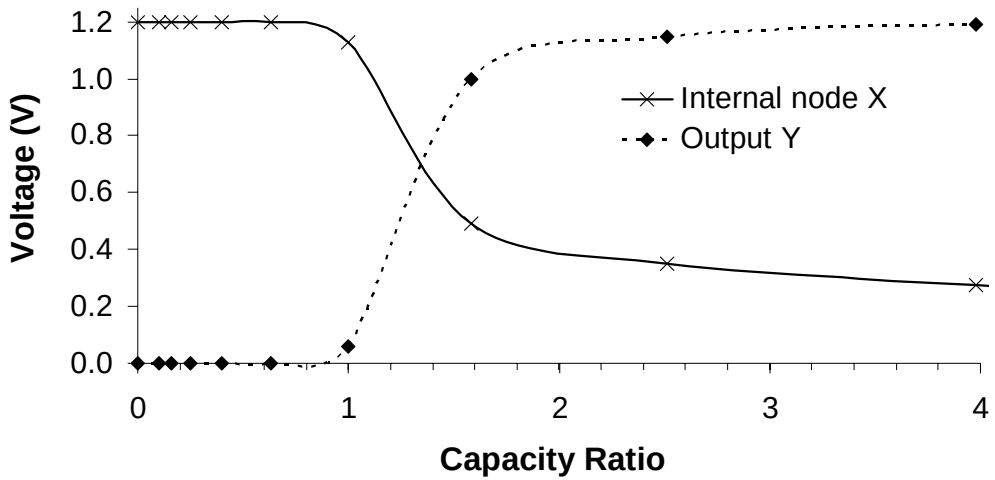
- Results for the worst-case scenario:
  - 90 nm Technology
  - Pipelined design (5 stages)
  - All gates with maximum wire load and maximum fan-out

Results

Reliability

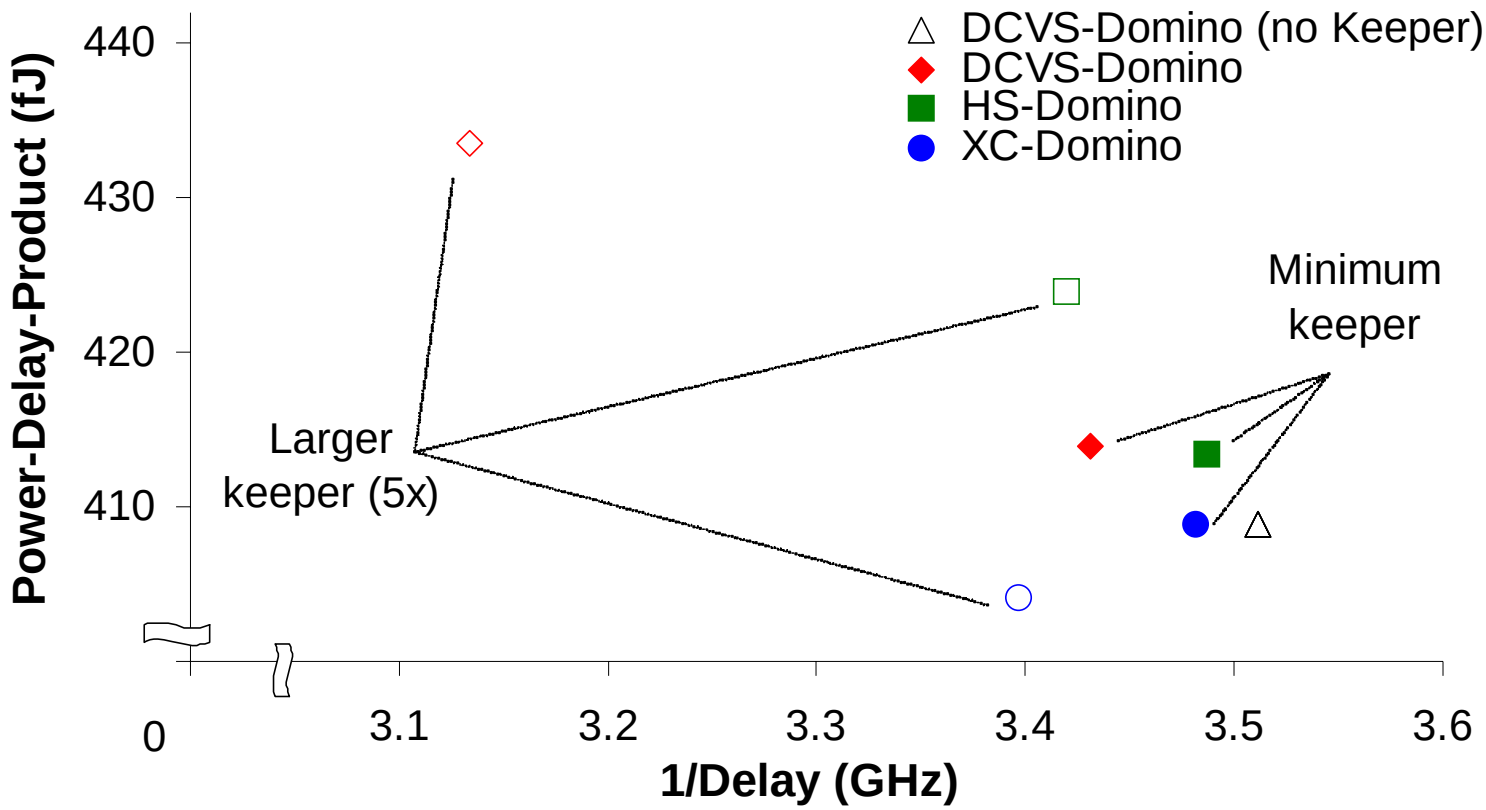
Large number of causes endangers reliability:

- Charge leakage
- Charge sharing
- Power supply noise
- Crosstalk
- Clock skew
- Substrate charge injection
- Soft errors
- and more **...**



$$\text{Capacity Ratio} = \frac{\text{PDN's internal capacitance}}{\text{Capacitance of the dynamic node}}$$

Results

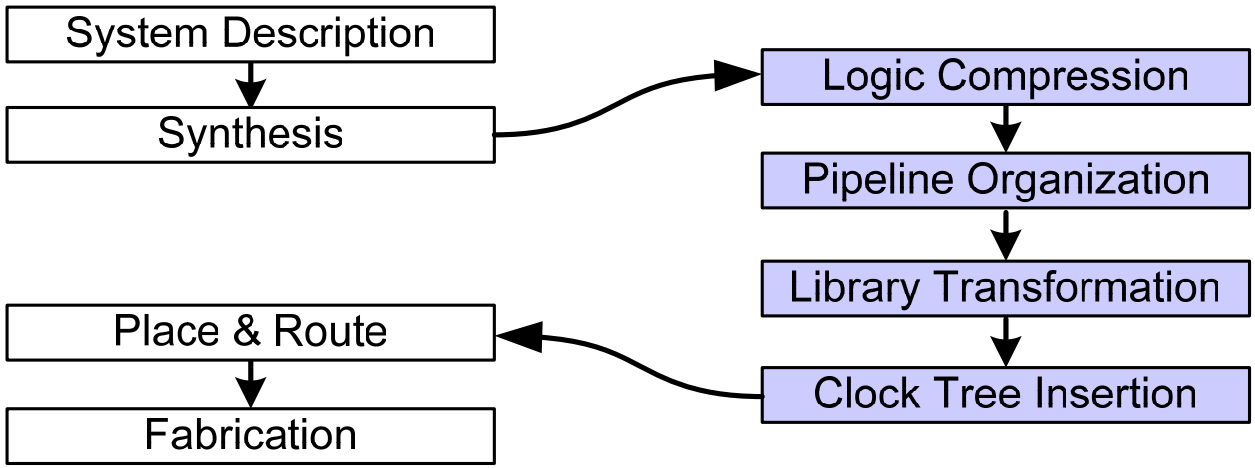


- Results for the worst-case scenario:
  - 90 nm Technology
  - Pipelined design (5 stages)
  - All gates with maximum wire load and maximum fan-out

Results

Design flow

- Automated design flow
  - Derived from standard CMOS flow
  - Logic compression for target library
  - Insertion of registers
  - Clock tree implementation



[Flügel, 2001]

Conclusions & Outlook

- Dynamic logic is functional in 90 nm technology
- Clearly outperforms static CMOS
  - in terms of delay and area @ high speed
- Reliability endangers signal integrity and has to be monitored

- Various dynamic logic styles applicable

Several techniques to cope with problems have become standard and ease the use of dynamic logic?

- Shadow latches, razor techniques
- Clock- and data-gating
- Dynamic Voltage/Frequency Scaling
- ...