Joint consideration of performance, reliability and fault tolerance in regular Networks-on-Chip via multiple spatially-independent interface terminals

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Abstract—The work at hand presents the evaluation results of an adapted mesh-based topology for Networks-on-Chip (NoC) operating via multiple spatially independent network interfaces in order to connect the computational resources of many-core systems. It can be shown that such minimal changes in comparison to standard two-dimensional meshes allow for significant improvements regarding network saturation and packet delay. At the same time, the resulting penalties for total power dissipation and area overhead of the NoC can be kept at moderate levels. Furthermore, the inherent dual-path capabilities with higher communication locality help to improve NoC fault tolerance as well as the thermal wear-out behavior. (Abstract)

Keywords—Networks-on-Chip; topology; many-core; dual-path routing; wear-out; fault-tolerance (key words)

I. INTRODUCTION

Networks-on-Chip (NoCs) emerged as the next generation of communication infrastructures for modern many-core systems applying packet-based communication inside a networked topology of routers interconnected by bidirectional point-to-point links [1]. The most commonly used NoC topology is the two-dimensional \( N_X \times N_Y \) mesh (2D-mesh) reverting to XY-routing and wormhole-switching. This abets regular physical layout, simplicity, scalability and the required degree of parallelism [2]. Typically, each computational resource is served by one dedicated router. In many cases, routers are enhanced by complex techniques like dual-path routing (e.g. XY/YX-routing), the utilization of virtual-channels (VCs) and deepening of the logical router pipeline by additional stages [2] in order to improve system performance.

In contrast, the quadrant-based mesh (QMesh) NoC proposed in this work simply connects each computational resource to the routers of all adjacent quadrants labeled Q0, Q1, Q2 and Q3 resulting in four connections at most. Thereby, the average hop distance of routing paths is reduced, dual-path routing is implemented without using VCs and traffic interferences are prevented more efficiently. Furthermore, the basic structure of the 2D-Mesh with all of its advantages including simple deterministic XY-routing is preserved.

The remainder of this paper is organized as follows. In section II related work on existing approaches is highlighted. In section III the QMesh topology is introduced. In section IV experimental results are summarized and discussed. Finally, in section V the work at hand is concluded and an outlook for future investigations is provided.

II. RELATED WORK

Different proposals favoring multi-ported NoCs and focusing on improvements regarding selected criteria can be identified. The DMesh [3] integrates two disjoint networks, where one network is responsible for traffic to/from the left section and the other for traffic to/from the right section relative to the source position. Furthermore, routers are connected diagonally via additional links. Hence, the DMesh suffers from structural irregularity and additional costs. Another approach using two spatially independent Network Interfaces (NIs) to improve fault tolerance is presented in [4]. However, the independent dual-paths are only provided for source-destination pairs along the same Y coordinate. The NR-Mesh [5] exhibits the same topological structure and connectivity as applied by the QMesh. Additionally, a probabilistic terminal selection for packet injection/ejection with distributed adaptation at each source is integrated. Furthermore, the NR-Mesh is proposed to work with two VCs. Thereby, hardware costs are approximately doubled when compared to the QMesh and deterministic traffic flows are prohibited. The MEPI-Mesh [6] uses a NI strategy similar to the NR-Mesh. However, the NIs (up to four at most) are interconnected via an intra-tile network and only one NI acts as master serving the computational resource directly. Forwarding packets to/from the remaining NIs is done via the intra-tile network. Thus, the master NI is a central bottleneck and the intra-tile network introduces additional delays.

III. QUADRANT-BASED MESH TOPOLOGY

The basic structure of the QMesh topology is illustrated in Figure 1 showing a 4x4 NoC. Furthermore, two source-destination pairs (SRC\(_{1/2}\) to DST\(_{1/2}\)) are depicted to highlight the dual-path options using XY-routing. Generally, packet injection into the 2D-mesh can be done at different routers depending on the relative position of the destination. Routing path information is derived from a path table resulting in two reasonable alternatives for every possible source-destination pair. Once injected, packets are forwarded following rules for
regular XY-routing until the destination router denoted in the path table is reached. This requires a simple XY-coordinate scheme for unique addressing within the 2D-mesh. Since the QMesh allows for the injection/ejection of packets via different routers placed around the source/destination, routing information comprises the input quadrant at the source (Q_IN), the XY-coordinates of the destination router and the appropriate output quadrant (Q_OUT) at this router to address the correct computational resource. Thus, addressing in packet headers must be extended by 4 additional bits for Q_IN and Q_OUT (each 2 bits). The required routing information is derived from a programmable path table (PT), which is integrated at each QMesh tile and represents the fundament for dynamic path updates. The PT overhead for each tile is expected to be negligible (e.g. 32/128 byte for 8x8/16x16 sized NoCs compared to kByte-sized transmission buffers per tile [7]). In comparison to the 2D-mesh, resulting path lengths are reduced by up to two hops, router-to-router links are disburdened from nearest-neighbor traffic and router traffic load is reduced.

IV. EXPERIMENTAL RESULTS

For experimental evaluation the QMesh (see Table 1 for parameter settings) is integrated into a cycle-accurate SystemC-based simulator [8] considering traffic-load-driven thermal impacts for both routers and links. Figure 2 illustrates the parameters serving to compare the 2D-mesh and the QMesh regarding relative improvements of network saturation (Δ_SAT), packet delay reduction (Δ_DELAY) and power overhead (ΔPOWER). Moreover, thermal related wear-out at minimum/maximum packet injection rates (a_MTTF at PIR_Low/High) is analyzed. This is done for 4x4 and 8x8 NoCs using various synthetic traffic patterns (transpose, bit complement, bit reverse, shuffle, random uniform, rentian, nearest-neighbor, and hotspot [1] [2] [9]). The rentian power-law distributed pattern produces network traffic comparable to benchmark applications like PARSEC with exponents of R=0.3 and R=0.7 as corner-cases over the majority of applications [9] [10]. The hotspot cases simulate 8 hot tiles along the NoC perimeter receiving 20%, 40%, 60% and 80% of NoC traffic to cover intense communication scenarios. All presented results represent the mean values over 10 simulation runs.

Furthermore, fault tolerance against uniformly injected random router failures is evaluated for the 2D-mesh and a modified 2D-mesh with up to four tiles per router (called CMesh) with and without XY/YX-routing. Results are compared to the QMesh applying dual-path XY-routing.

![Figure 1: Example of a 4x4 QMesh topology](image)

![Figure 2: Basic parameters for experimental evaluation](image)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Link width</td>
<td>64 bits / 8 bytes</td>
</tr>
<tr>
<td>Router port buffer depth</td>
<td>9 flits / 72 bytes</td>
</tr>
<tr>
<td>Topology</td>
<td>2D-Mesh, CMesh, QMesh</td>
</tr>
<tr>
<td>Switching</td>
<td>Wormhole</td>
</tr>
<tr>
<td>Routing</td>
<td>XY</td>
</tr>
<tr>
<td>CMOS technology</td>
<td>45 nm [13]</td>
</tr>
<tr>
<td>NoC frequency</td>
<td>1 GHz</td>
</tr>
<tr>
<td>Packet size (random uniform)</td>
<td>20% with 2 flits / 16 bytes</td>
</tr>
<tr>
<td></td>
<td>80% with 9 flits / 72 bytes</td>
</tr>
<tr>
<td>NoC operation time</td>
<td>5 ms</td>
</tr>
</tbody>
</table>

Table 1: NoC simulation parameter setup

![Figure 1: Network saturation impact of the QMesh](image)
The QMesh clearly outperforms the 2D-mesh regarding $\Delta_{\text{SAT}}$ with up to 105% and 29%/36% on average over all 4x4/8x8 traffic scenarios (see Figure 3). Packet delay reductions $\Delta_{\text{DELAY}}$ amount to 78% in maximum and 53%/48% on average over all 4x4/8x8 scenarios (see Figure 4). At the same time, the total power overhead $\Delta_{\text{POWER}}$ averages out at 45%/53% over all 4x4/8x8 scenarios (see Figure 4). Thermal related wear-out improvements $a_{\text{MTTF}}$ amount to a factor of 2.3 in maximum and 1.6/1.3 on average (see Figure 5). In general, the acceleration factor $a_{\text{MTTF}}$ determines the temperature-related increase or decrease of wear-out progress for CMOS devices [12] (see Equation 1). Therein, $t_{\text{QMesh}}$ and $t_{\text{2DMesh}}$ specify the mean-time-to-failure (MTTF) of the QMesh and the 2D-mesh component. $E_a$ is the activation energy in electron volts (0.7 eV at 45nm CMOS [11]), $k$ is the Boltzmann’s constant (8.6×10^{-5} eV/K) and $T_{\text{QMesh}}$ and $T_{\text{2DMesh}}$ describe the absolute temperatures in Kelvin per router/link resulting from the simulated traffic load of the NoCs (bit-toggle rate of 0.5 assumed).

$$a_{\text{MTTF}} = \frac{t_{\text{QMesh}}}{t_{\text{2DMesh}}} = e^{\frac{E_a}{k} \left( \frac{1}{T_{\text{QMesh}}} - \frac{1}{T_{\text{2DMesh}}} \right)}$$ (1)

In none of the widespread scenarios the QMesh is outperformed by the 2D-mesh. The total NoC area footprint increases by around 78% (45nm CMOS) due to the utilization of eight-ported routers in the QMesh, while the XY-routing 2D-mesh only requires five ports per router. In comparison to the XY/YX-routing 2D-mesh with two VCJs and dual-path capabilities, the area overhead of the QMesh shrinks to 7.7%. All power and area values were explored using DSENT [12].

Furthermore, the dual-path QMesh features a significantly higher degree of fault tolerance for up to 16 faulty routers inside an 8x8 NoC. This is attributed to the spatially independent paths, beginning and ending at different NIs, maintaining a higher degree of end-to-end connectivity (see Figure 6) as well as resource availability (see Figure 7) than the evaluated reference cases.

In detail, Figure 6 shows the relative amount of the average remaining end-to-end connections per tile over the variation of inserted router faults. As it can be seen, the QMesh outperforms all reference cases in the presence of router failures. Furthermore, Figure 7 depicts the relative fraction of reachable tiles over the variation of router faults. While both 2D-mesh and CMesh lose at least one tile with each faulty router, the QMesh benefits from its spatially independent NIs offering the best degradation characteristics.

Figure 2: Degradation of end-to-end connectivity over variation of router failures

V. CONCLUSION AND FUTURE WORK

The results indicate that simple design decisions, such as the number and placement of resource interface terminals, can result in synergistic effects improving major run-time characteristics of many-core systems. Nevertheless, the major assets of 2D-meshes can be preserved.
The presented work is the initial step in order to provide software-managed NoCs supporting improved characteristics regarding communication locality, performance, fault tolerance and wear-out. The introduced programmable path tables offer a unified interface for traffic management at the inter- and intra-tile level over a wide range of scenarios \[13\] \[14\]. Therefore, the next step is the integration of monitoring capabilities for traffic management from existing approaches that were already explored for the 2D-mesh \[15\] \[16\]. The combination with mechanisms for error and fault management would create a holistic software-based management service.

REFERENCES


