Reduction of Power Dissipation in *Deep Submicron* Designs

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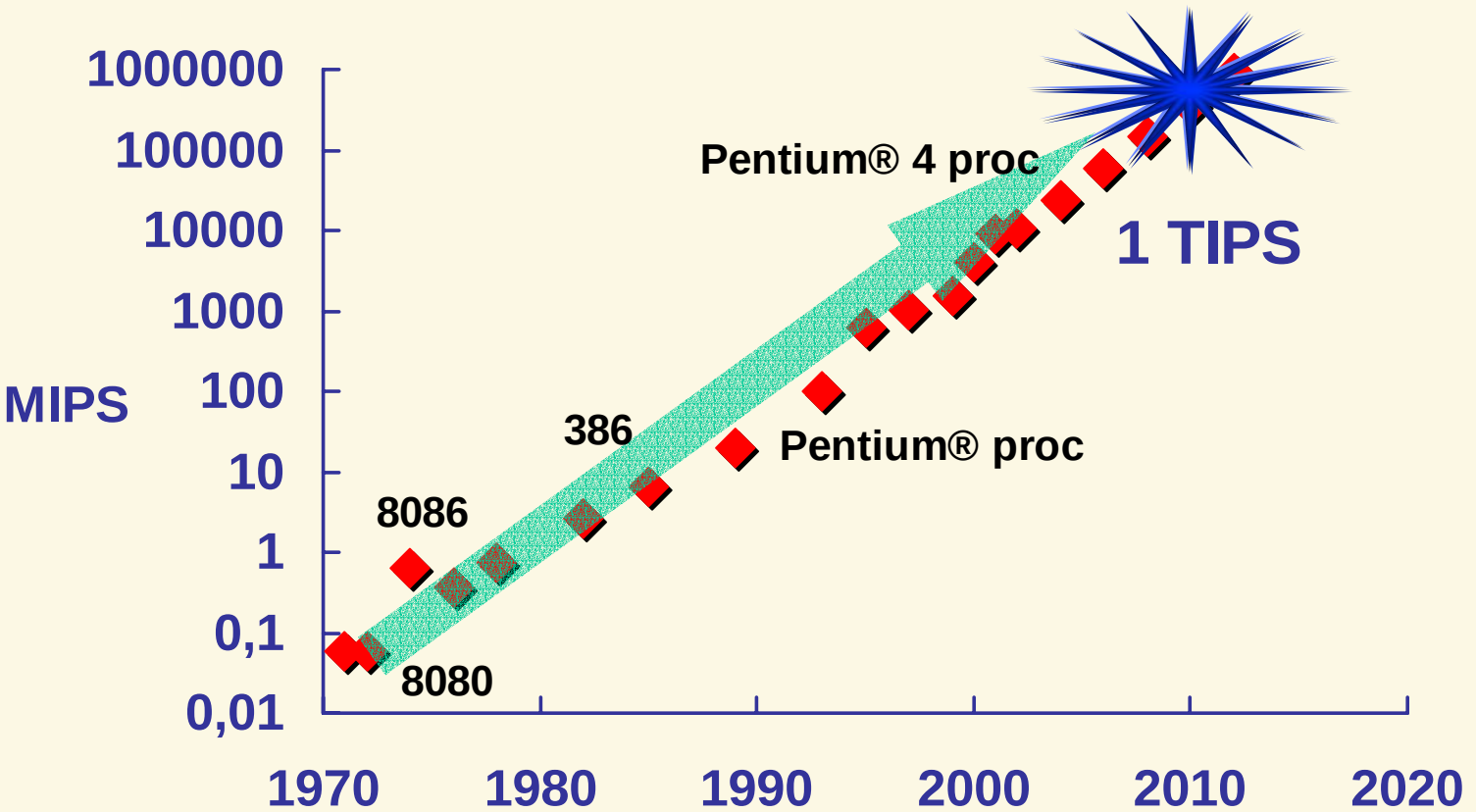
Outline

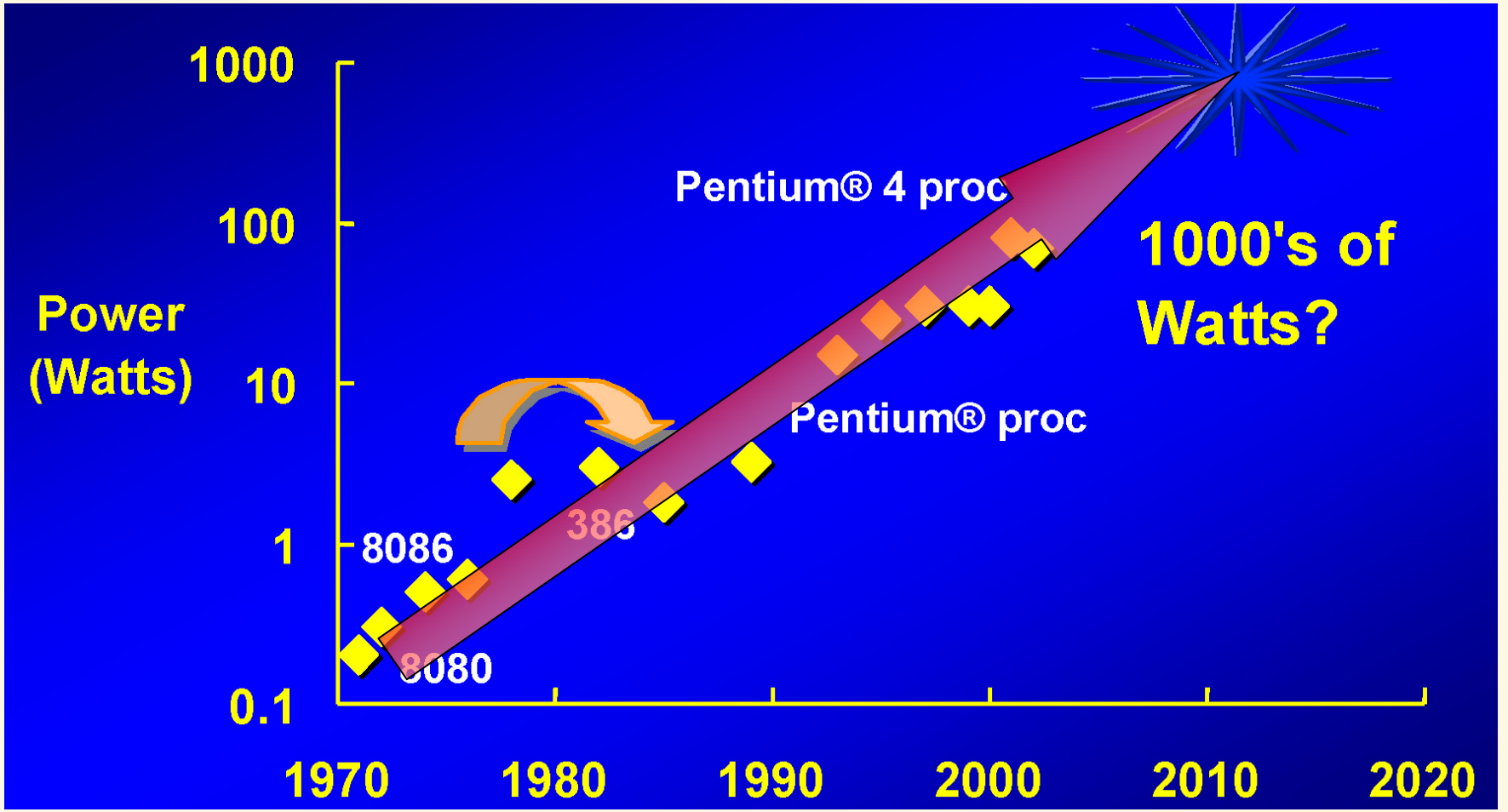
1) Power dissipation in *deep submicron* designs
2) Basics
3) Approaches to reduce power dissipation
4) Summary

Trend: Performance



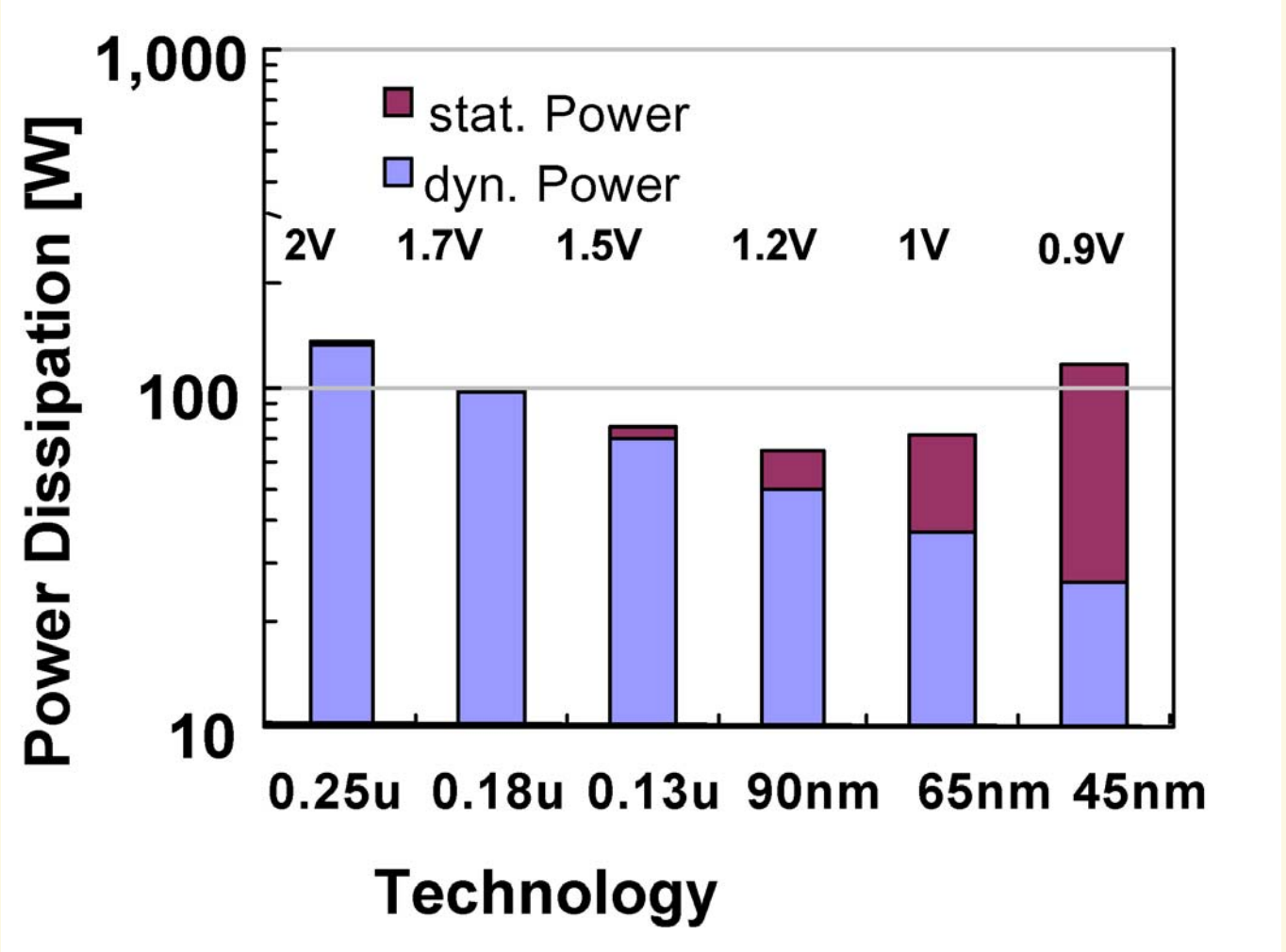
Intel, ‘03

Trend: Power



Intel, '03

Dynamic Power vs. Leakage

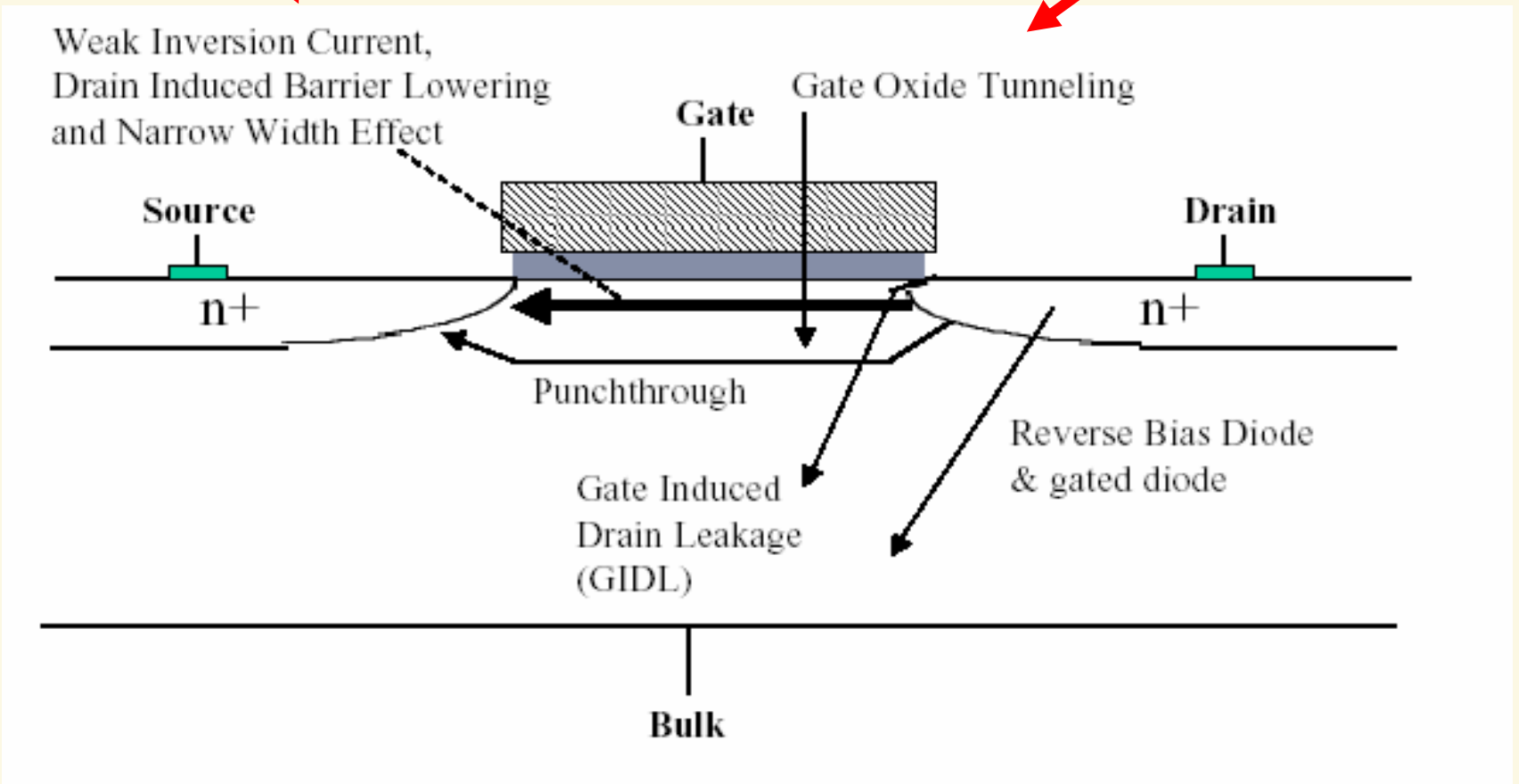


Intel, '02

Contributions to Leakage

dominates

increases fast



Power & Delay dependence

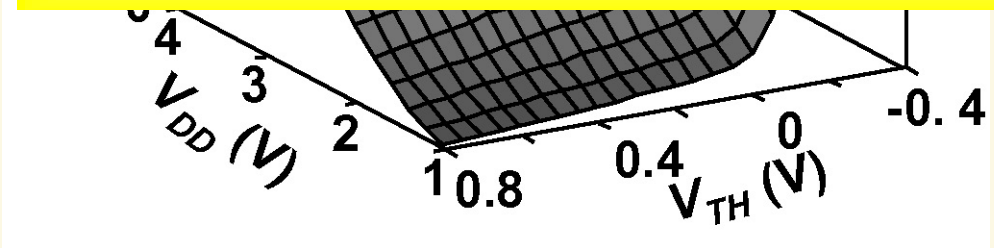
$$P = p_t \cdot f_{CLK} \cdot C_L \cdot V_{DD}^{\ 2} + I_0 \frac{W_T}{W} \cdot 10^{\frac{-V_{TH}}{S}} \cdot V_{DD} \qquad t_d = \frac{k \cdot Q}{I} = \frac{k' \cdot C_L \cdot V_{DD}}{(W/L) \cdot (V_{DD} - V_{TH})^{\alpha_K}}$$

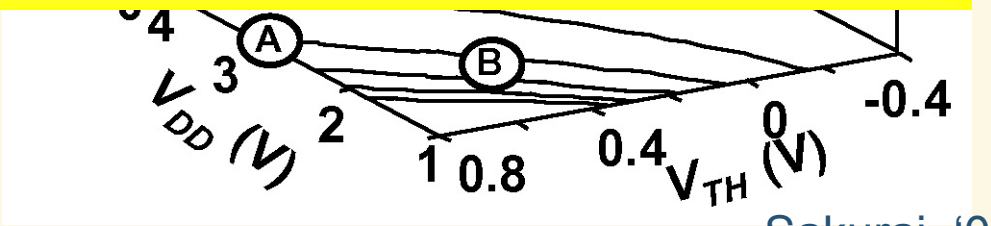
Problem:

fast transistors with high power dissipation (low V_{th})

or

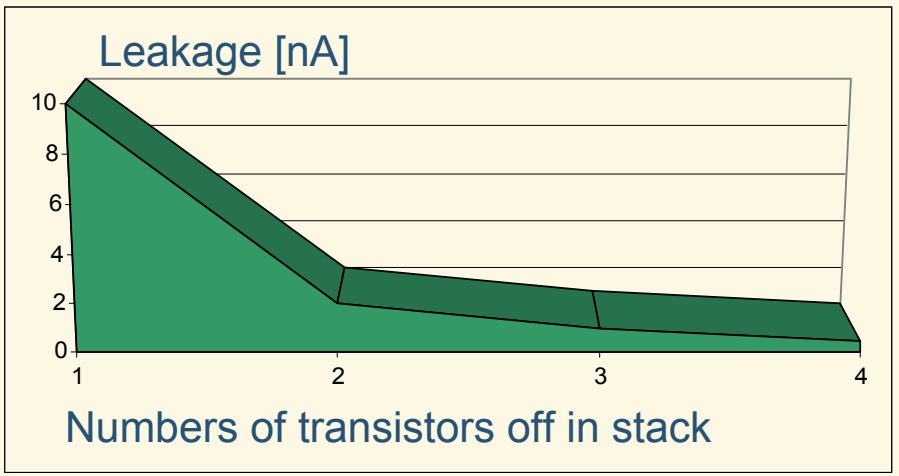
slow transistors with low power dissipation (high V_{th})

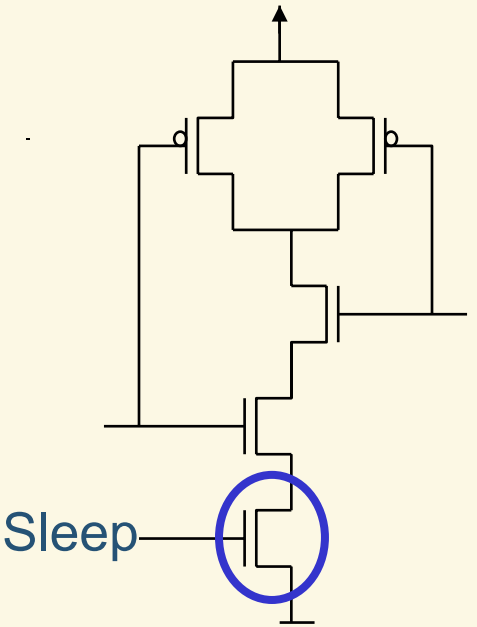




Sakurai, '01

Approach 1: Sleep - Transistor





Insertion of transistors with high-V_{th} in path to GND

→ blocking in sleep mode

➡ reduced static power dissipation in sleep mode

Approach 2: Pin Reordering

- I_{sub} depends on the *number* of OFF in stack
- I_{gate} depends on the *position* of ON/OFF transistors

NAND3:

Inputs	I_{gate} in [nA]	I_{sub} in [nA]	I_{total} in [nA]
011	6,774	1,522	**8,295**
101	3,720	0,761	4,481
110	3,720	0,000	**3,720**

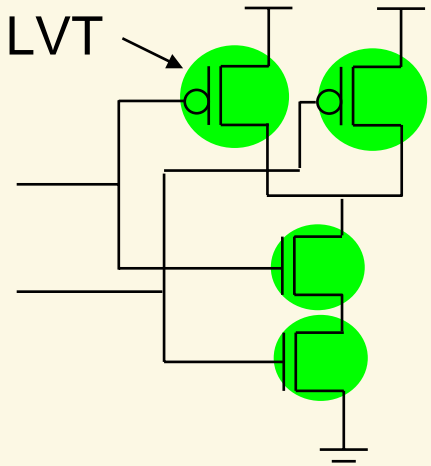
→ Pin with highest '0 – probability' → bottom transistor to reduce leakage!

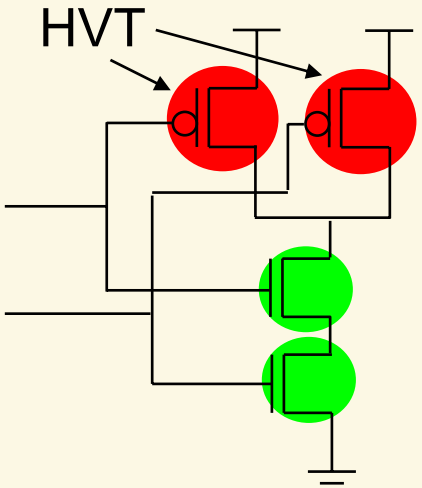
New Approach: Mixed - VT (MVT) CMOS

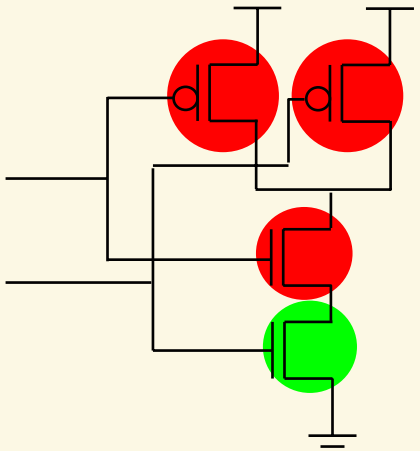
Goal: cells keep the delay while leakage decreases

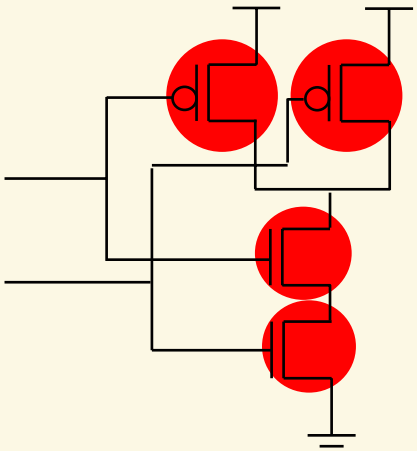
- if all transistors in cell are equal dimensioned → different output slopes
- up to now: dimensioning of transistors
- new Idea: use different threshold voltages within a cell

MVT- NAND2



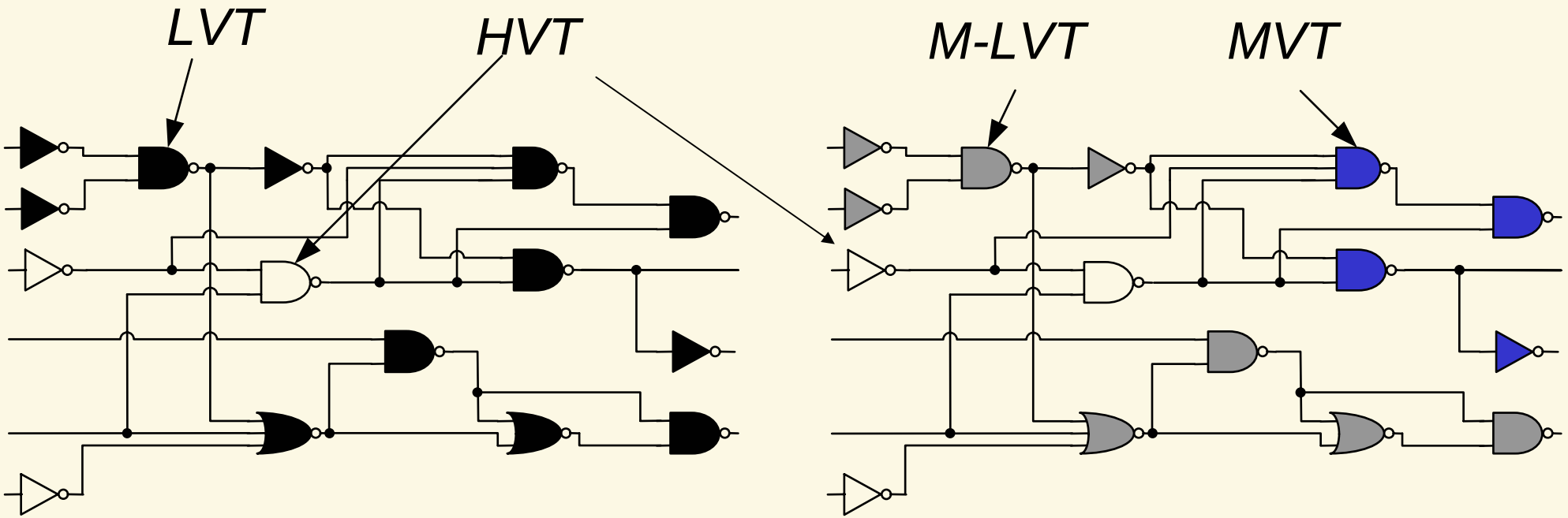






***LVT* cell**	***M-LVT* cell**	***MVT* cell**	***HVT* cell**
- all MOS have low V_{th}	- PMOS have high V_{th}	- PMOS and upper NMOS have high V_{th}	- all MOS have high V_{th}
- rise time is shorter than fall time	- rise and fall time are nearly the same	- middle delay cell	- maximum delay cell
- minimum delay cell	- minimum delay cell		

MVT - Paths



Up to now: *two kinds of cells*
(Dual-Threshold CMOS)

MVT-CMOS

Summary

- Static power dissipation is an increasing problem
- Sub-threshold and gate-leakage currents dominate
- Reduction of leakage power by:
  - additional sleep transistors
  - Reordering of pins
  - different threshold voltages