SRD – Towards a System for the In-Situ Detection of the Stapedius Reflex

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***Abstract*—Cochlea implants help regain the auditory sense in cases where the cochlea has lost its ability to transform incoming sound signals into electrical stimulation for the auditory cortex. A cochlea implant requires a first calibration process, which is often based on the well-known stapedius reflex. This paper proposes a system, called the stapedius reflex detector (SRD), that aims to provide a step towards the automatic in-situ exploitation of this reflex. A first prototype has been implemented on a field-programmable gate array. The first validation experiments indicate that the system is properly working and ready for further development that aims to integrate this system into the clinical process.**

I. Introduction

No doubt, the auditory sense plays an important role in the personal communication of humans. But unfortunately, this sense might be progressively degrading due to age, injuries, and other reasons [1]. In such cases, hearing devices are common means for a relief: by providing a frequency-selective amplification of the sound signal, they help regain at least parts of this important sense.

By their very nature, hearing devices fail, if too many hair cells of the cochlea are destroyed. In such cases, cochlea implants [2] can be the last resort. In essence, a cochlea implant consists of a small number of electrodes, which are inserted into the cochlea and which can electrically stimulate the hair cells that connect to the auditory cortex. The implant's electrodes receive their stimulation input from a signal processor, which analyzes the incoming sound signals. Section II provides a brief description of the cochlea implants in the context of the human ear as far as necessary for the understanding of this paper.

A major issue during the implantation of a cochlea implant is its first proper calibration [3]. The goal of this initial calibration is to adjust the implant's parameters, which are mainly the frequency-specific gain factors, such that the auditory system receives as much stimulation as possible without causing any stimulation overload. This calibration process becomes particularly problematic for persons who have never gained any auditory experience, since they cannot give any useful feedback to the medical staff.

In many clinics, the initial calibration process of the cochlea implants is based on the *stapedius reflex*, which refers to the activation of the *stapedius muscle*: In case the auditory system receives too much stimulation [4], e.g., high-volume music, it activates this muscle, which reduces the mobility of the auditory ossicles which in turn imposes an additional damping of the perceived sound signal. The very purpose of this reflex is to prevent the auditory system from any damage, and is thus associated with pain within the brain [5]. The advantage of this reflex is that it can be exploited during surgery at the open ear by visual inspection. But the difficulty is that with a length of about 7 mm, the stapedius muscle is the smallest one in the human body and that it is quite hidden in the ear.

As mentioned above, the stapedius reflex has so far been exploited by visual inspection. This inspection, however, is neither easy to perform, nor is it applicable in the every-day life situation. Because of these limitations, Section III proposes a new architecture, called the stapedius reflex detector (SRD). SRD aims to provide a step towards the following three goals: (1) the in-situ detection of the stapedius reflex, (2) the implementation as an embedded system with the option of being integrated into a hearing device or into the cochlea implant, and (3) providing a means for the online adaptation of the implant's parameters. By processing the electrical data derived within the stapedius muscle, the first version of the SRD system focuses on the detection of the stapedius reflex.

Due to lack of experience and available research data, the requirements, particularly with respect to the computational resources, for such a system are not clear yet. Therefore, the first experimental system designs were not made with a conventional (signal) processor in mind. Rather, a field-programmable gate array (FPGA) was chosen as a research and development platform. An FPGA is a general-purpose hardware device that consists of about 5,000 to 500,000 freely configurable logic elements. By using high-level hardware description languages, such as VHDL [6] or Verilog [7], the programmer can create arbitrary system hardware designs, and can easily integrate complex modules, such as an entire soft-core processor. Section IV discusses how to implement the core parts of the SRD system on a standard, off-the-shelf FPGA.

The first prototype of the SRD system was used in a series of experiments. The results of these tests are summarized in Section V, and include some validation tests as well as the analysis of pre-recorded clinical data. The results indicate that

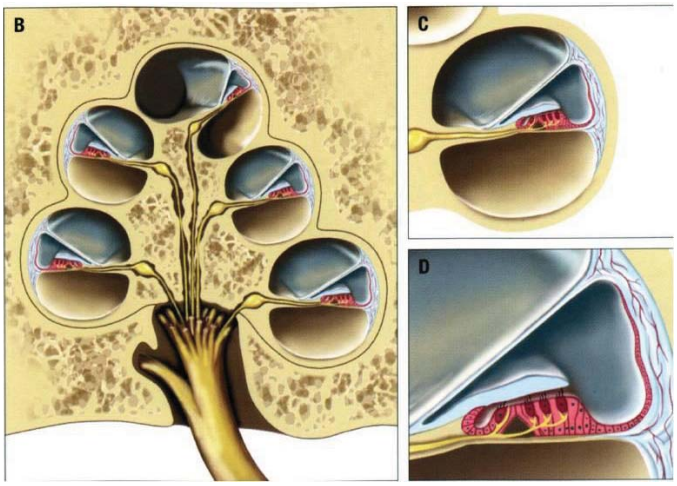

Figure 1. B truncated cochlea. C cochlea profile with three floors: Scala vestibule, Scala media, Scala tympani. D Enlargement of C

the system is properly working and ready for the integration into the clinical process; this integration, however, requires further development steps. Finally, Section VI concludes this paper with a brief discussion. This discussion includes an outline of the next research and development steps that are required for a proper integration of the SRD system into the regular clinical process.

II. Background: Human Ear and Cochlea Implants

This section has three main purposes: (1) a brief review of the human ear, (2) a short illustration of the stapedius reflex, and (3) a short description of how cochlea implants work.

A. The Human Ear

The human ear is quite a complex organ and consists of the outer, middle, and inner ear [8]. The outer ear is the part that is visible from the outside and that consists of the ear piece and the auditory canal. The middle ear consists of three bones that are also known as malleus, incus, and stapes, which are the smallest bones of the human body. The ear drum separates the outer from the inner ear, and provides a mechanical connection between them. Finally, the inner ear is made off the cochlea and the auditory nerv that connects to the auditory cortex.

The outer ear protects the inner parts from damage, and provides a direction-sensitive characteristic that helps estimate the direction under which a sound source appears. Once a sound signal has entered the outer ear, it makes the ear drum vibrate accordingly, since sound signals are longitudinal waves.

The three ossicles of the inner ear merely forward the vibrations from the ear drum to the inner ear. In so doing, however, it increases the vibration's force (and, of course, decreases its amplitude). They thus perform an impedance change for the next processing stage, the inner ear's cochlea.

The cochlea (Fig. 1) is quite a complex organ, which is packed as a slug. Roughly speaking, the cochlea consists of two long tubes that are closely attached to each other by the Reissner's membrane. One of these tubes is filled with a water-like liquid, which is stimulated by the middle ear's stapes. The other side of Reissner's membrane hosts the basilar membrane, which employs a large number of hair cells. These hair cells connect to the auditory cortex via the auditory nerve. In short, the ossicles's vibrations propagate from the cochlea's liquid to the hair cells, which in turn perform a transformation from mechanical energy into electrical stimuli, which are finally send to the auditory cortex [4].

B. The Stapedius Reflex

In the signal propagation chain described above, the hair cells play an essential role. But these hair cells can be irrecoverably damaged, if the cells are exposed too long to high-energy noise. Once the hair cells' hairs are broken (off), they cannot transform mechanical into electrical energy, and consequently, the brain cannot properly hear even though all the other components of the auditory path are still in operation.

For the protection of the hair cells, the human brain features a "safety mechanism", also called *stapedius reflex*: The middle ear's stapes is connected to the *stapedius muscle*, which is about 7 mm in length. In case the auditory cortex receives too much stimulation, due to too much sound energy, the cortex triggers the reflex, which lets the stapedius muscle contract. This contraction increases the damping along the ossicles, and thus, the damping of the sound signal.

It might be interesting to note that the hair cells are damaged not only by too much exposure to noise, e.g., loud discotheques and construction zones, but also by age and birth defects. The latter are particularly problematic, since they severely hinder the children's social and intellectual development.

C. Cochlea Implants

Cochlea implants are common means to bridge improperly working hair cells. Figure 2 shows that a cochlea implant consists of two major parts: (1) a speech processor, which is attached to the outer ear, and (2) an electrical stimulator, which stimulates the hair cells by means of a small number of electrodes. Both parts are connected with each other by a pair of wireless communication modules, called transmitter and receiver. These modules allow for the communication through the skin.

The signal processing starts off at the speech processor. It receives the acoustic signal by means of a tiny microphone. It then calculates a frequency-specific stimulation, which it sends to the transmitter, which is essentially a simple coil. On the other side of the skin, an electrical receiver transforms the signal into specific electrical pulses, which are used by the electrodes to stimulate the hair cells. This electrical stimulation is forwarded to the auditory cortex as usual.

Since a cochlea implant works *in situ*, its effectiveness depends, among other things, on the electrical characteristic of the electrode-to-cell surface. Therefore, a cochlea implant requires a first calibration, which is normally done during surgery by visual inspection of the stapedius muscle.

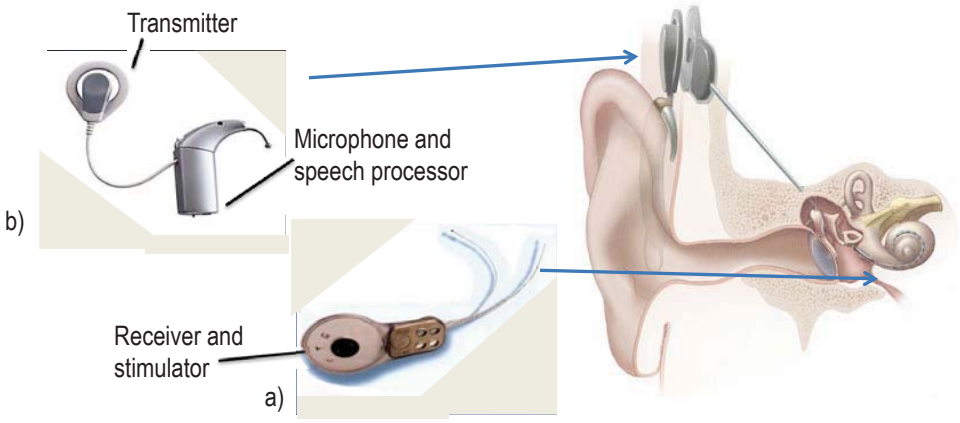

Figure 2. The components of a cochlea implant: (a) inner part, (b) outer part

In addition, an implant's effectiveness might change over time. This might be due to certain adaptation processes at the electrode-to-cell surface and due to a permanent too low or too high an acoustic stimulation. These factors already require a sporadic readjustment of the frequency-specific gain factors, which normally takes place in the speech processor.

III. SRD – The Stapedius Reflex Detector

A. Data and System Requirements

The procedure during surgery has already been explained: after inserting it, the implant is stimulated with a 1,500 Hz signal, and the gain is increased until the stapedius reflex can be visually observed.

In order to make a step forward towards the automatic, online detection of the stapedius reflex, the surgeon also inserts a bipolar hook electrode into the stapedius muscle. The data that is derived by means of these electrodes is recorded by an intramuscular electromyography recorder, and visualized in Fig. 3. The EMG signal is bandpass filtered with cut-off frequencies 10 Hz and 2 kHz. This signal is the power amplified and digitized with 5128 Hz sampling rate and 12 bit resolution. Since the procedure requires approximately

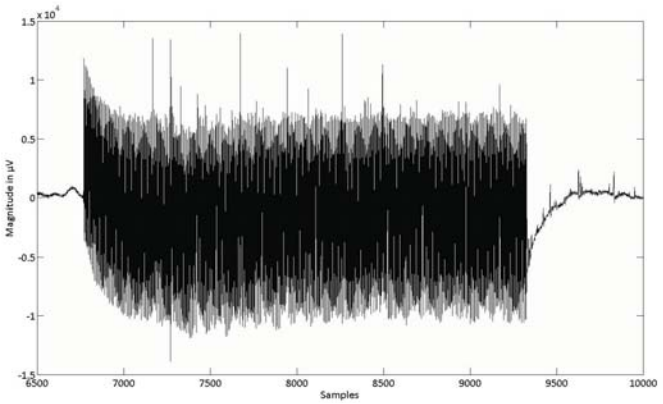

Figure 3. This figure shows the data that is derived at the stapedius muscle during an external stimulation of the cochlea.

2 s, such a detector system should be able to process at least 15,000 bytes, which may be temporarily stored, e.g., for performing a fast fourier transform (FFT).

B. System Architecture

The top-level view of the SRD architecture is shown in Fig. 4. It consists of an analog-to-digital converter (ADC), an embedded soft-core processor, e.g., a Nios II processor [9], a bandpass filter to remove any noise from the raw data, and an evaluation unit. The evaluation unit may consist of adequate computations, such as an FFT or a bank of bandpass filters, which are discussed in Subsections III-C and III-D.

The ultimate goal of the SRD system is to provide an automatic detection of the stapedius reflex. This purpose does not require any data storage. However, for documentation purposes as well as supporting further research, the entire data set should be stored on the system. After the implantation, this data may be transfered to a host system via a dedicated link (not shown in Fig. 4).

C. Realization Variant: FFT

A fast fourier transform (FFT) would probably be the most common way to analyze data, such as those presented in Fig. 3. To this end, the first system variant employs the Radix-2 FFT algorithm [10] on the internal processor.

The advantage of this technique is that it is well established and that sample implementation code is freely available. However, a drawback of this approach is that the data has to be stored on the system, at least temporarily. For a resolution of 0.6 Hz and a frequency spectrum of nearly 0 Hz-2,500 Hz, this approach requires at least enough memory of internal RAM for one frame of 8192 samples. Further memory requirements may be considered, if the processing speed is too slow and/or if the overlapping of the windows is to fine grained.

D. Realization Variant: Filter Bank

The main result of an FFT is the power spectrum of a signal. In other words, the FFT determines what frequencies are present in the signal and what their (relative) amplitudes are. The same result can also be achieved by a collection of

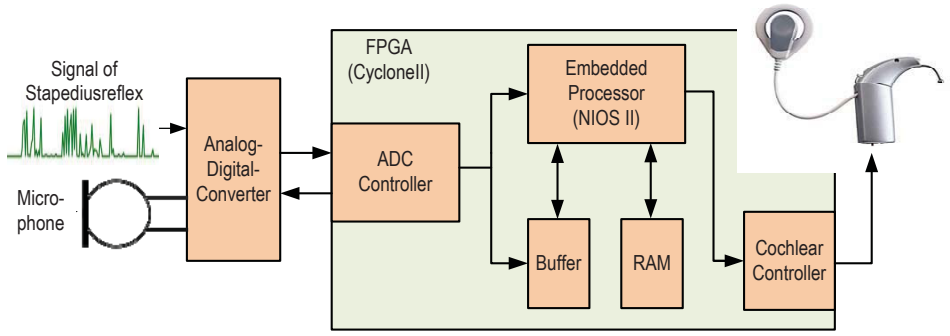

Figure 4. The top-level view of the SRD architecture.

bandpass filters. A bandpass filter is a sequence of a low pass filter and high pass filter, and lets pass only those frequencies that are within the specified cut-off frequencies.

In the context of a digital system, most programmers are certainly inclined to an FFT analysis for very good reasons. One of these reasons is that on a *sequential computer*, an FFT is much faster than the simulation of a large number of bandpass filters. However, hardware platforms, such as field programmable gate arrays, do allow for a one-to-one realization of such filters. That is, all the filters can be processed in *parallel* at hardware speed. An interesting side effect is that one bandpass filter requires only four bytes of memory multiplied by its order. Most filters are at most of third order, and thus require only 12 bytes. Furthermore, a small number, e.g., 10-100, of bandpass filters would suffice for the detection of a stapedius reflex.

A bank of bandpass filters would also have another advantage: rather than a sequence of a low pass and a high pass filter, a bandpass filter can also be constructed by two low pass filters. In that case, the output is simply the difference of both low pass filters multiplied by a constant gain factor. In case of a regular structure, two bandpass filter can always share one low pass filter, which significantly reduces the system requirements. This architecture is illustrated in Fig. 5.

The SRD prototype considers both implementation variants in order to explore their particular advantages and disadvantages in the problem at hand.

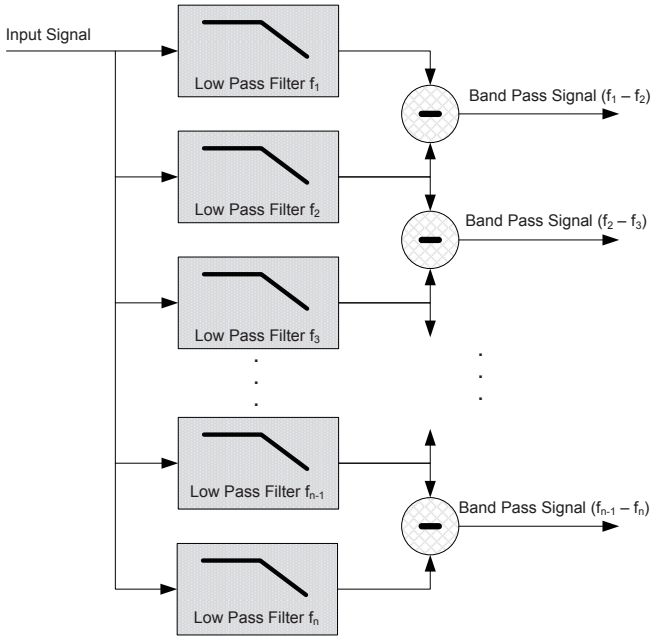

Figure 5. This figure shows how a bank of bandpass filters can be constructed out of a cascade of low pass filters. In this approach, every pair of bandpass filters share one low pass filter.

IV. An FPGA-based Prototype Design

For the first prototype, an Altera Cyclone II FPGA [11] was chosen. This device offers 33,216 logic elements and can be clocked at about 85 MHz. Because of its resources, this devices offers enough options for research and development. Furthermore, the available simulation, synthesis, and debugging tools provide excellent development support. In addition, standard components, such as the Nios II soft-core processor can be integrated by simply "drag-and-drop".

For the first SRD variant, a standard implementation of the FFT could be easily ported onto the Nios II. With the chosen configuration of 1024 data points per FFT and a window shift of 512 data points, the Nios II requires 4.7 s computation time per second of data input. That is, the Nios II is five times too slow to keep up the data input speed, and its performance would linearly degrade if the window shift decreases, which would be desirable, for a faster response. This performance figure indicates that a Nios-II-based FFT is too slow for an online, in-situ analyzer. Therefore, future implementation should consider a commercially available hardware FFT realization, which requires about 4000 logic elements and would charge about 500 USD.

For the second variant, an additional filter bank was also realized on the same FPGA. In order to retain the inherent parallelism, this filter bank was not computed within the Nios II processor, but was directly realized in hardware. The implementation of a single low pass filter in VHDL is as simple as in the following *sample code*:

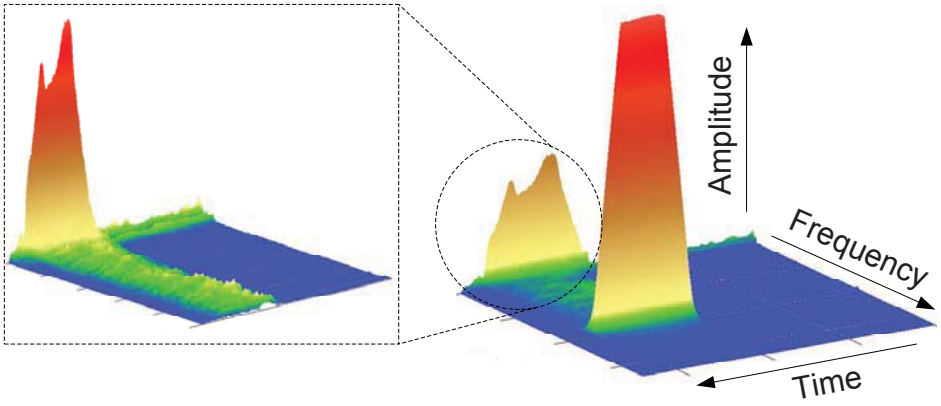

Figure 6. This figure shows the result of the FFT on the data presented in Fig. 3.

```
calc_filter: process( ... )

-- old_output, new_output, input are
   the architecture's logic vectors

-- local declarations
variable tmp1, tmp2, tmp3, tmp4:
             signed(31 downto 0);

begin -- process calc_filter
  tmp1 := signed(old_output)
  tmp2 := SHIFT_RIGHT(signed(old_output),
                      FILTER_SHIFT);
  tmp3 := SHIFT_RIGHT(signed(input),
                      FILTER_SHIFT);
  tmp4 := tmp1 - tmp2 + tmp3;
  new_output <= std_logic_vector(tmp4,
                                 WIDTH);
end process calc_filter;
```

This sample code is a little simplified in that the architectural (context) signals are omitted. And the variables `input`, `old_output`, and `new_output` refer to the input value and the output values of the low pass filter at the previous as well as the subsequent time steps, respectively. A bank consisting of 20 first-order bandpass filters consumes merely 2000 logic elements, which is almost negligible.

V. Results

The first prototypical implementation of the SRD system has used the data already shown in Fig. 3. The data was sampled at 5128 Hz. Furthermore, the sampling utilized a power amplifier, since at the bipolar hook electrode, the maximum voltage is as small as 90 μV.

Figure 6 shows the result of the FFT with a window shift of 10 data points. The right-hand-side presents the entire spectrum of the data over the complete time interval. The stimulation at 1,500 Hz can be clearly seen. The left-hand-side of the figure magnifies the frequency range of 0 Hz to 500 Hz. This enlargement clearly shows that the stimulation of the cochlea implant leads to a significant change in the low-frequency part.

The second SRD realization variant was also used in the practical experiments. First of all, the filter bank was used in a series of synthetic data. The validation results are presented in Fig. 7. It can be clearly seen that the three bandpass filters, which were tuned to 500 Hz, 1500 Hz, and 2500 Hz, have the expected effect on a 500 Hz square-wave signal.

In addition, this variant was also applied to the recorded data. Figure 8 shows the original raw data already shown in Fig. 3 after processing with a bandpass filter with cut-off frequencies of 10 Hz and 500 Hz. Further filtering has shown the same qualitative behavior as the FFT did in Fig. 6. That is, the filter bank also indicates a pronounced activity in the low frequency range, if the cochlea implant is stimulated above a critical threshold. In other words, both systems yield the same qualitative results, but in different domains, i.e., the frequency spectrum and the time discrete filter outputs.

VI. Discussion

This paper has presented a system that makes a step towards the automatic online detection of the stapedius reflex. It has also been explained that this reflex can be used as the basis of the first calibration of a cochlea implant, since this reflex indicates that the acoustic signal has surpassed a critical threshold. In this view, the stapedius reflex detector (SRD) is a sensor that directly processes neurophysiological data in situ. And its output directly controls an implant that also operates in situ by its very nature. SRD is thus a technical sensor that connects bio feedback with an implant.

Currently, the SRD system exists in two implementation variants. The first one is a rather classical FFT-based system, whereas the other one resembles the mode of operation of the cochlea's hair cells: the narrow bandpass filters selectively respond to a narrow frequency range as the hair cells do.

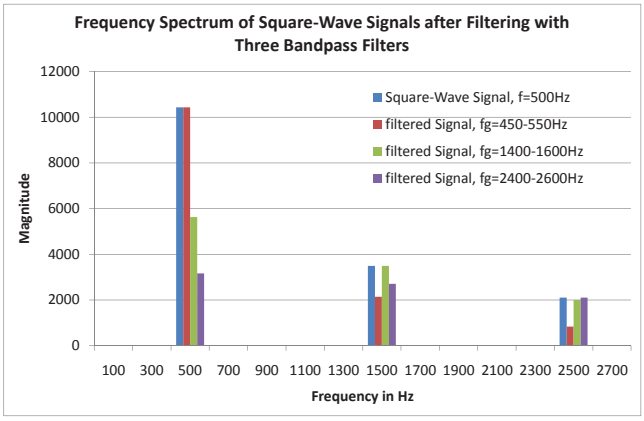

Figure 7. This figure shows the frequency spectra of a 500 Hz square-wave signal after filtering with three bandpass filters, which were tuned to 500 Hz, 1500 Hz, and 2500 Hz.

Both systems have their own merits. The first architecture can be implemented on any standard (signal) processor. The second one, by way contrast, is more tailored to fine-grained parallel hardware architectures, such as field-programmable gate arrays (FPGAs). Since this approach conserves the inherent parallelism, which is strictly sequentialized in an FFT, the overall system requirements are drastically smaller; the incoming data is being processed by a moderate number of simple processing elements, which have very low speed requirements. By contrast, the FFT-based approach requires quite a fast (signal) processors in order to respond in due time and in order to prevent the memory from being overloaded. The memory requirements are a further advantage of the second approach since there no external memory and therefore no memory controller is required.

Future research will be dedicated to the integration of the SRD prototype into the clinical process. This step requires further research, which includes: automation of the entire process, integration of the power amplifier, and finding suitable thresholds for the reliable detection of the stapedius reflex. These steps have to substitute the graphical data representation, which is currently done on the PC, by activating *one* single alert indicator.

Then, the first phase of clinical validation will also suggest a decision concerning which of the system variants is better tailored to the practical operation.

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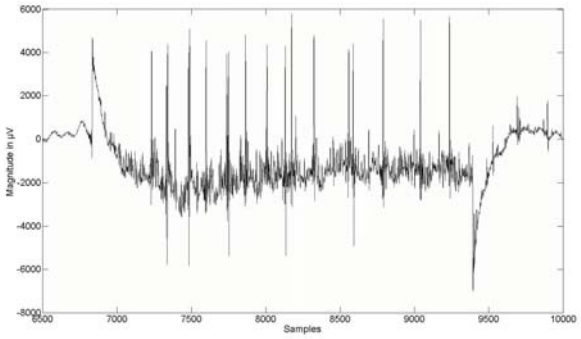

Figure 8. Result of filtering the raw data (see, Fig. 3) with a bandpass filter with a cut-off frequencies of 10 Hz and 500 Hz.

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