

ReCoSoC '06

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Mixed Gates: Leakage Reduction Techniques applied to Switches for on-chip Networks

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Focus of this Work

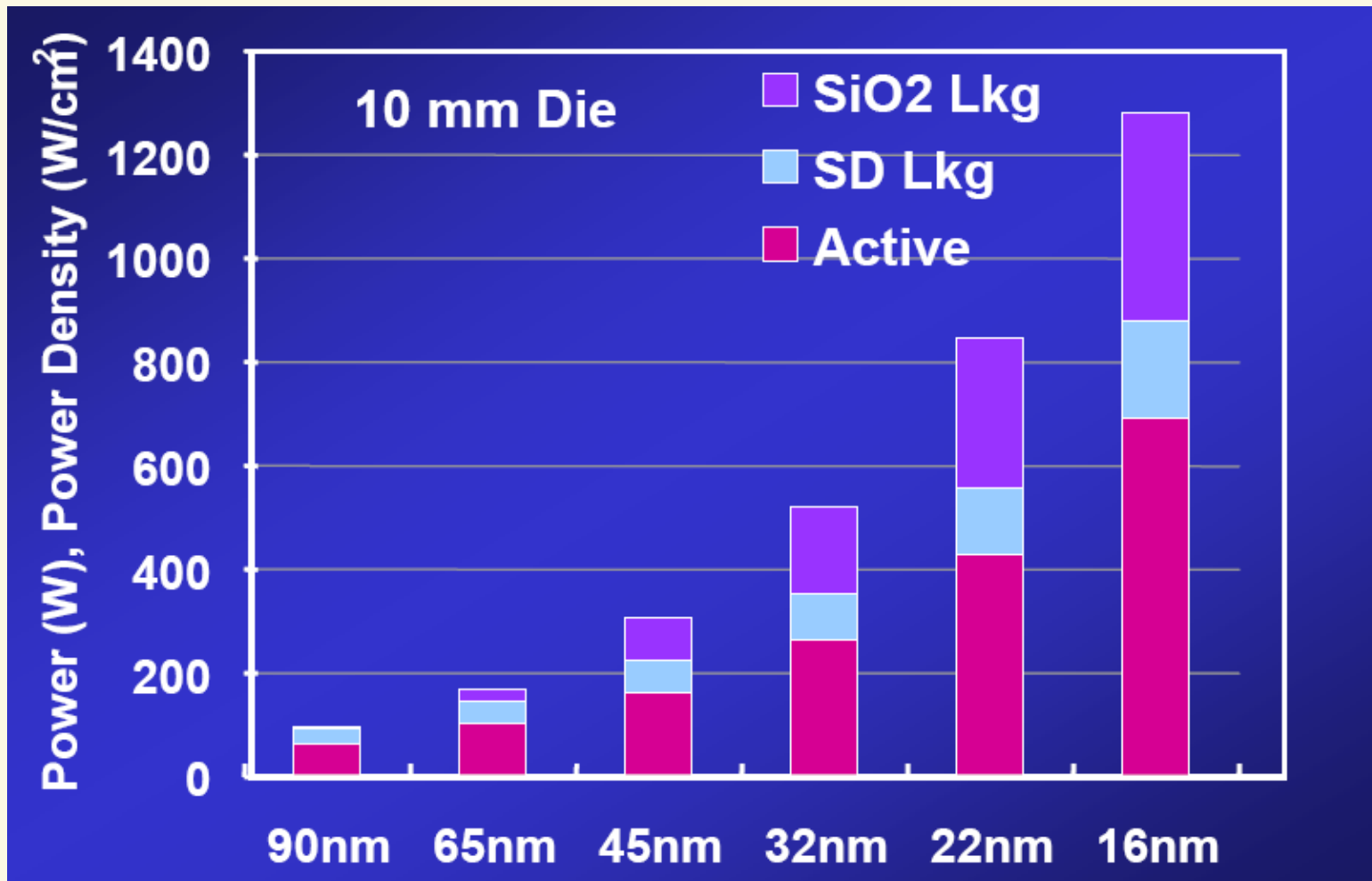
1. Advancement of established Leakage Reduction techniques (DVTCMOS / DTOCMOS)
2. Application of the new approach to NOC Switches

DVTCMOS:	Dual V_{th} CMOS
DTOCMOS:	Dual T_{ox} CMOS
NOC:	Network-On-Chip

Outline

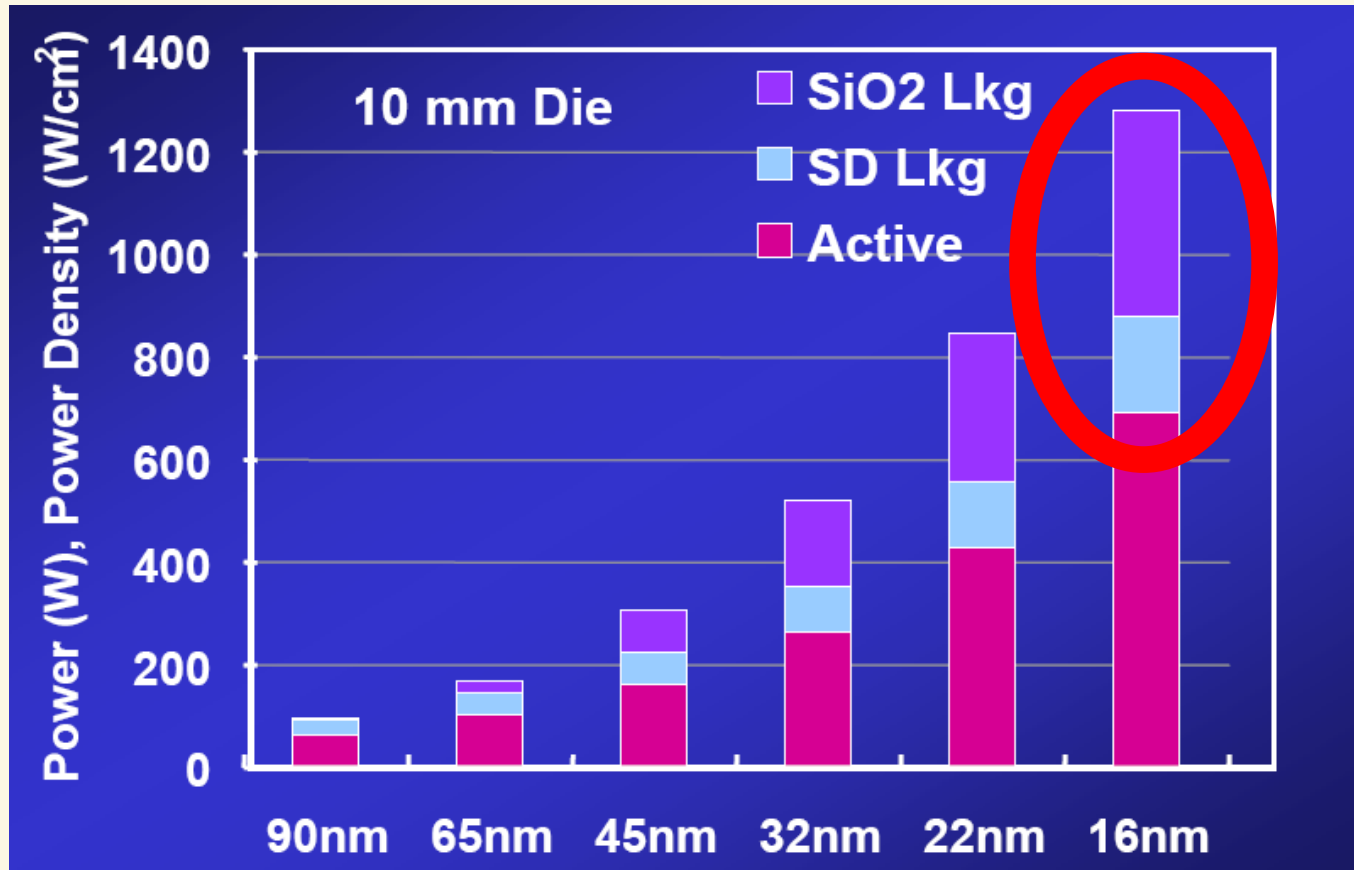
1. Motivation
2. Basics
3. Mixed Gates
4. Leakage Reduction of NOC Switches
5. Conclusion

Motivation



S. Borkar, '05

Motivation



Up to 50 %
will be
leakage!

SiO₂ Lkg - Gate Oxide Tunneling Leakage (I_{gate})

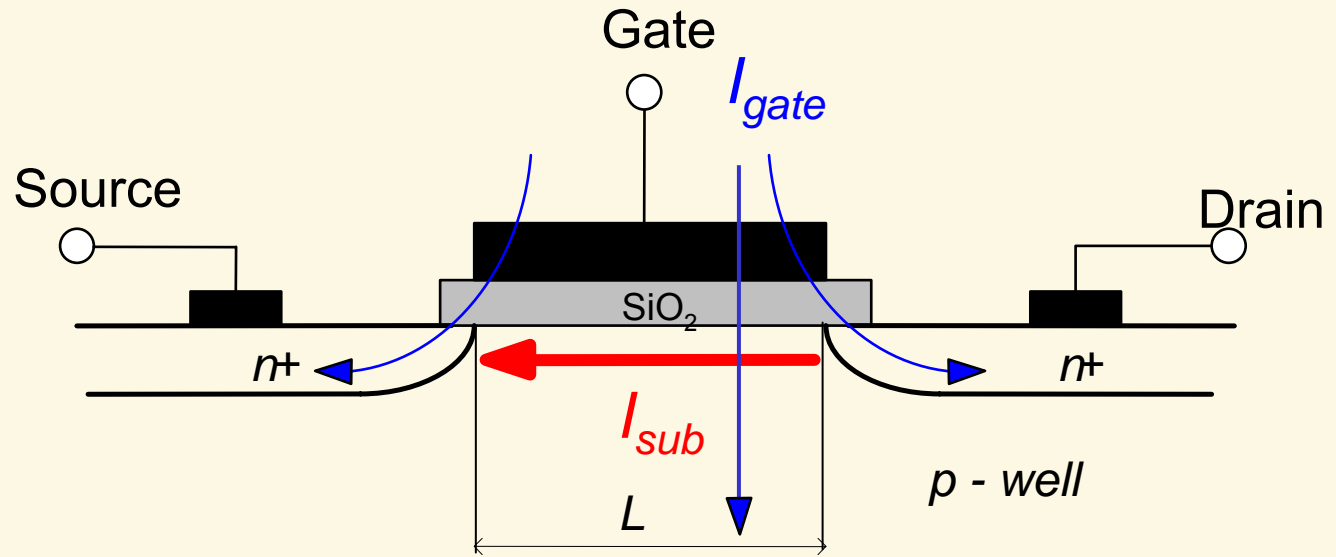
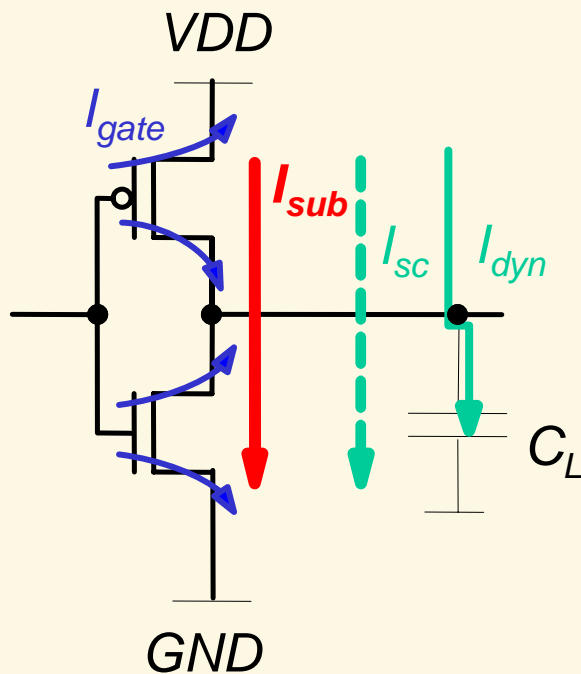
SD Lkg - Subthreshold Leakage (I_{sub})

S. Borkar, '05

2. Basics

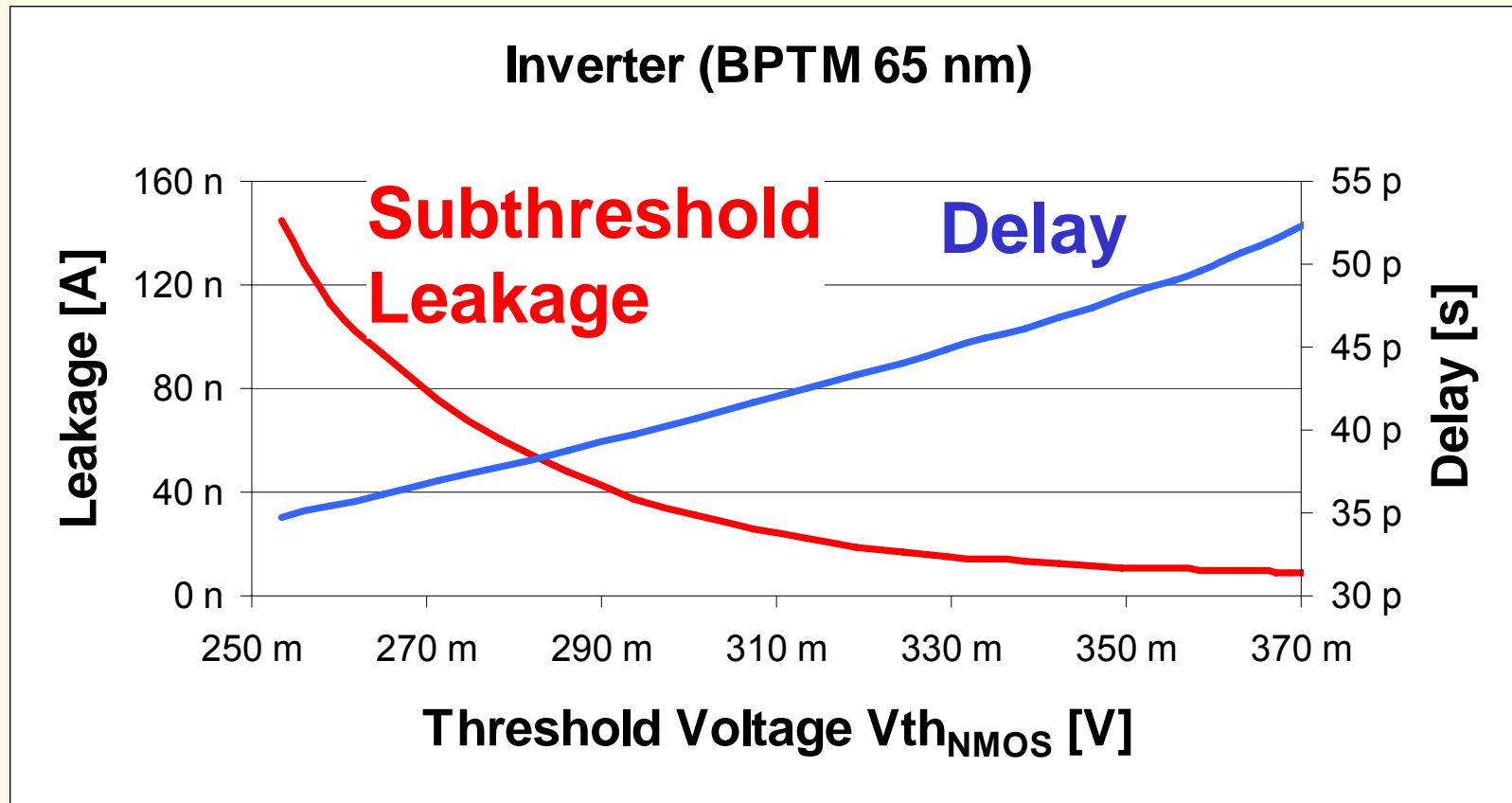


Power Dissipation in CMOS



- I_{sub} occurs if $V_g < V_t$
- carriers move by diffusion along surface
- I_{gate} caused by direct tunneling through gate oxide

V_{th} vs. Delay and Leakage



V_{th} vs. Delay and Leakage

fast devices with high power dissipation (low V_{th})

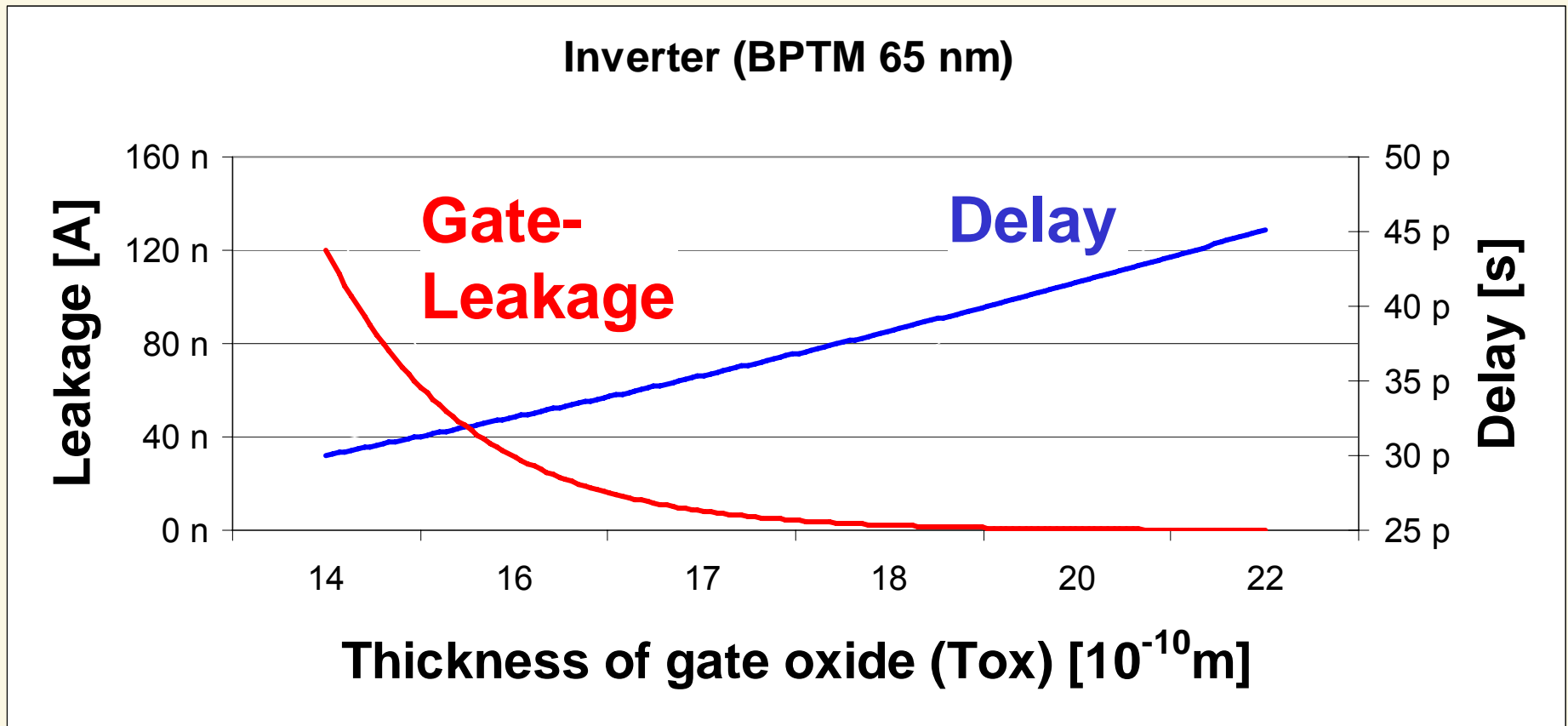
or

slow devices with low power dissipation (high V_{th})

200 mV 270 mV 200 mV 370 mV 300 mV 300 mV 370 mV

Threshold Voltage $V_{th_{NMOS}}$ [V]

T_{ox} vs. Delay and Leakage



T_{ox} vs. Delay and Leakage

fast devices with high power dissipation (low T_{ox})

or

slow devices with low power dissipation (high T_{ox})

Thickness of gate oxide (T_{ox}) [10^{-10} m]

DVTCMOS / DTOCMOS

Dual Threshold Voltages (DVTCMOS)

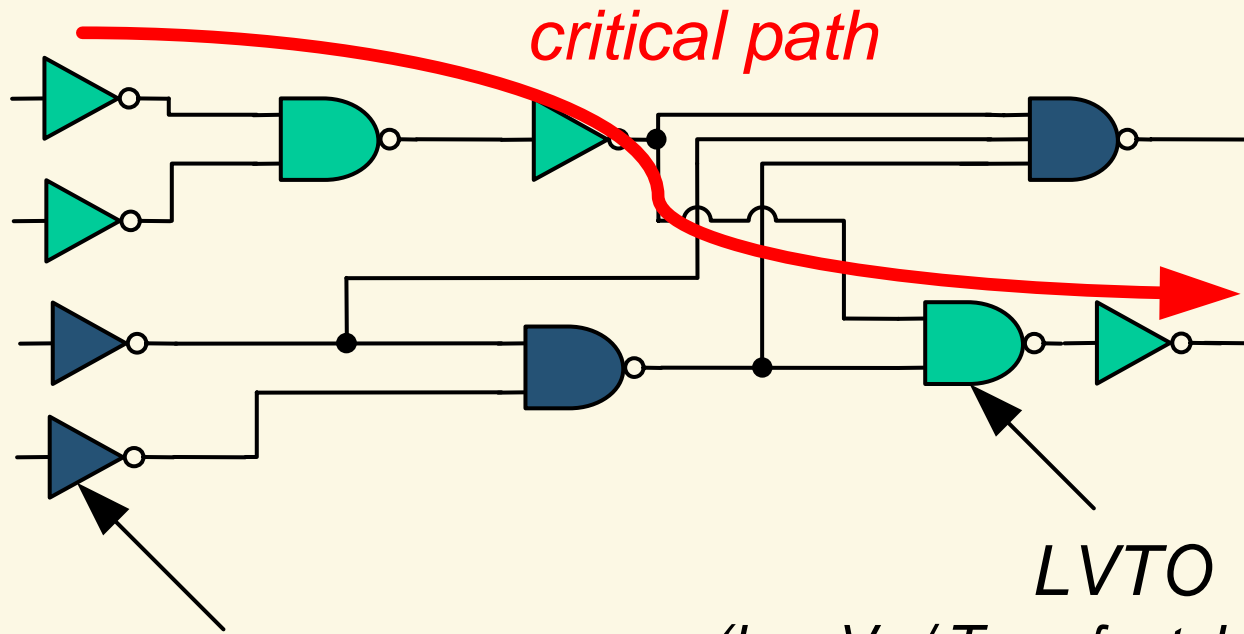
- Use different V_{th} 's
 - use **lower** threshold for devices **within** the critical paths
 - use **higher** threshold for devices **outside** the critical paths

Dual Tox (DTOCMOS)

- Use different T_{ox} 's
 - use **thinner** gate oxide for devices **within** the critical paths
 - use **thicker** gate oxide for devices **outside** the critical paths

 **Decrease leakage without performance penalty**

DVTCMOS / DTOCMOS cont'd



HVTO

(high V_{th} / T_{ox} = slow, low leakage)

LVTO

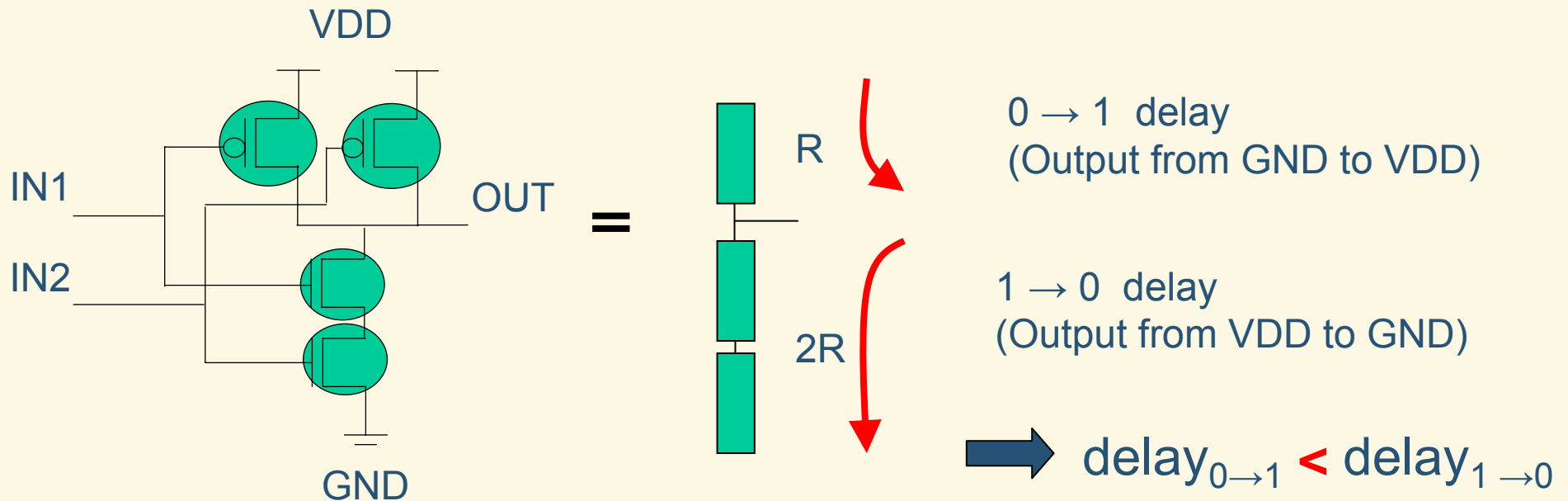
(low V_{th} / T_{ox} = fast, high leakage)

3. Mixed Gates



Mixed- V_{th}/T_{ox} Pull-Down/Up-Paths

Goal (for fast gates): Preserve the delay while decreasing the leakage

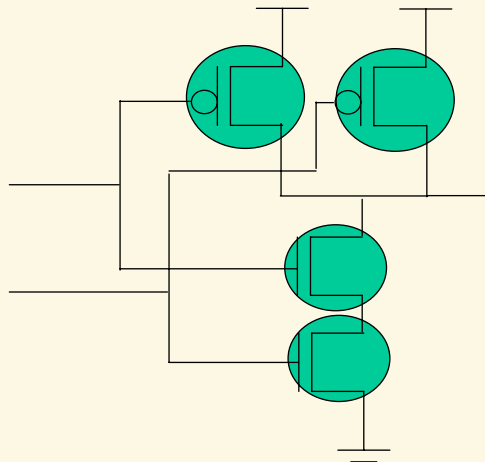


But: At timing analysis → only maximum delay is considered!

Mixed- V_{th}/T_{ox} Pull-Down/Up-Paths Cont'd



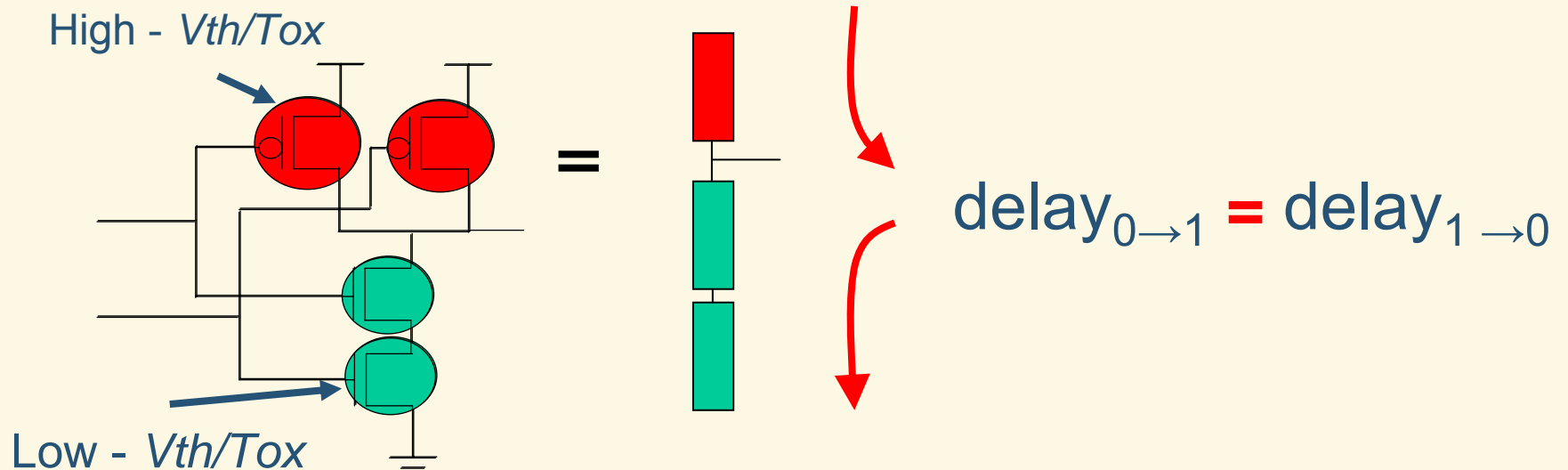
Idea: Use different V_{th} / T_{ox} devices within a gate to adapt the delays



Mixed- V_{th}/T_{ox} Pull-Down/Up-Paths Cont'd



Idea: Use different V_{th} / T_{ox} devices within a gate to adapt the delays



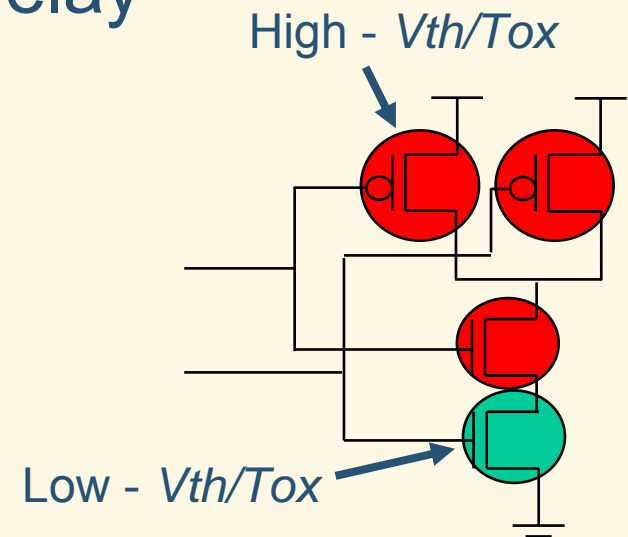
Mixed Gates

Goal: Additional gate types at constant mask count

Only two gate types in DVTCMOS / DTOCMOS

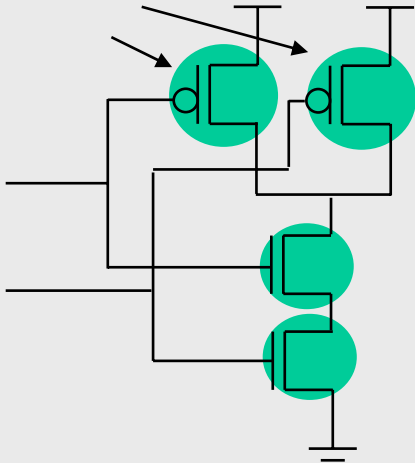
→ Problem: More *high leakage* gates after optimization as needed to keep the delay

➔ **Idea:** Mixed V_{th} / T_{ox} gates to increase the amount of possible gate types



Mixed Gates - NAND2

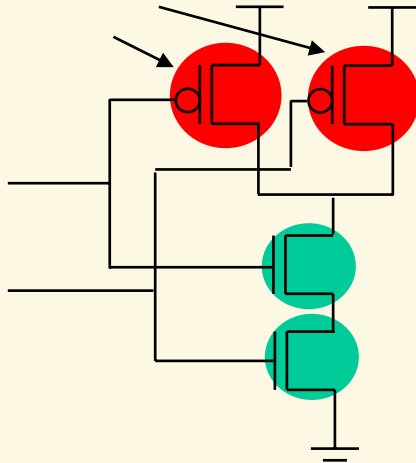
Low - V_{th}/T_{ox}



LVTO gate

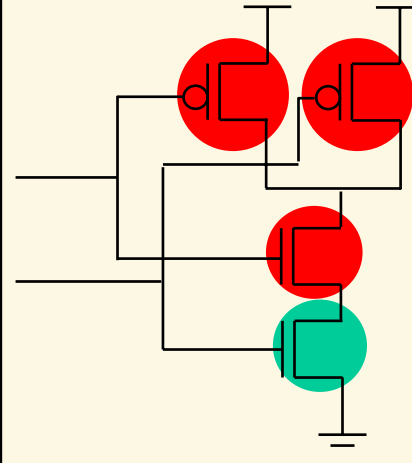
- rise time is shorter than fall time
- **minimum delay cell**
- **very high leakage**

High - V_{th}/T_{ox}



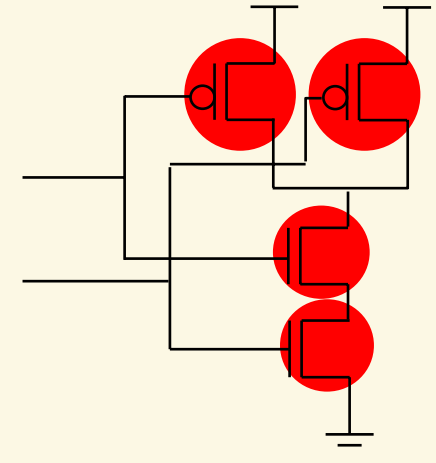
F - MG gate

- rise and fall time are nearly the same
- **minimum delay cell**
- **high leakage**



MG gate

- **middle delay cell**
- **middle leakage**



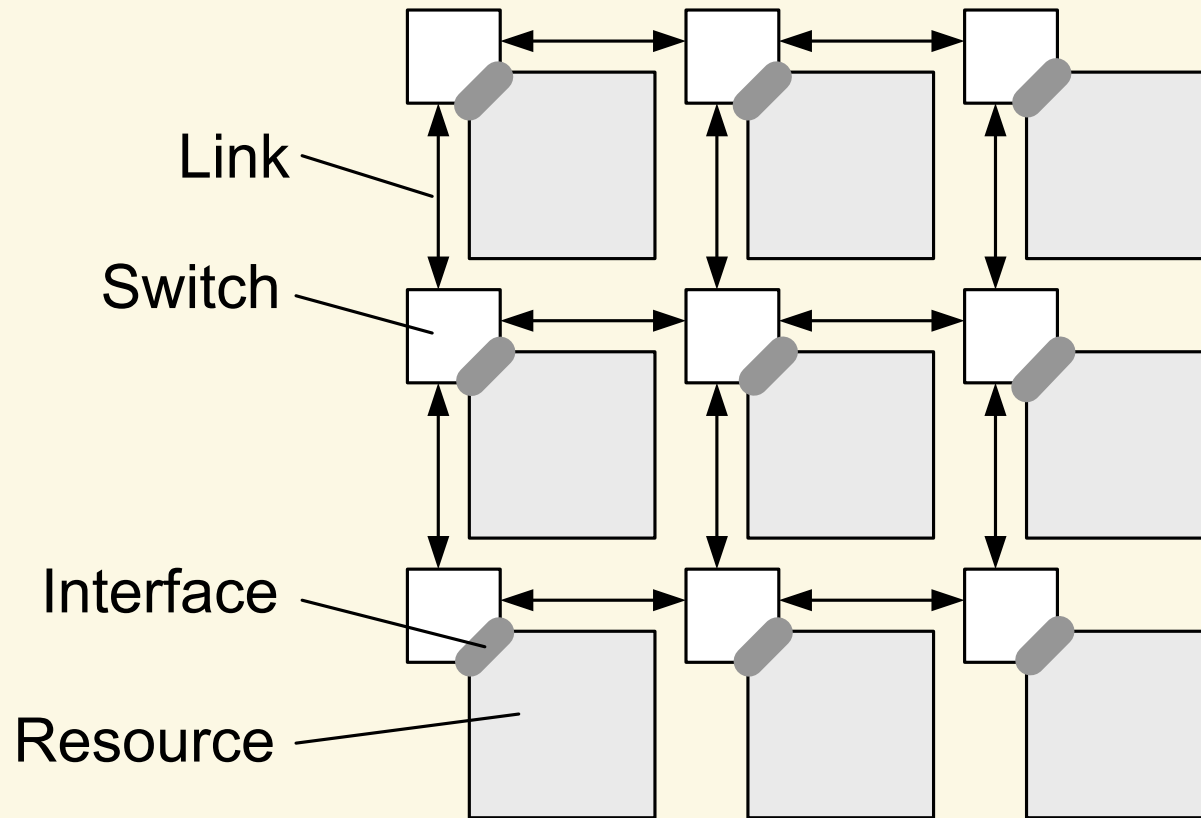
HVTO gate

- **maximum delay cell**
- **minimum leakage**

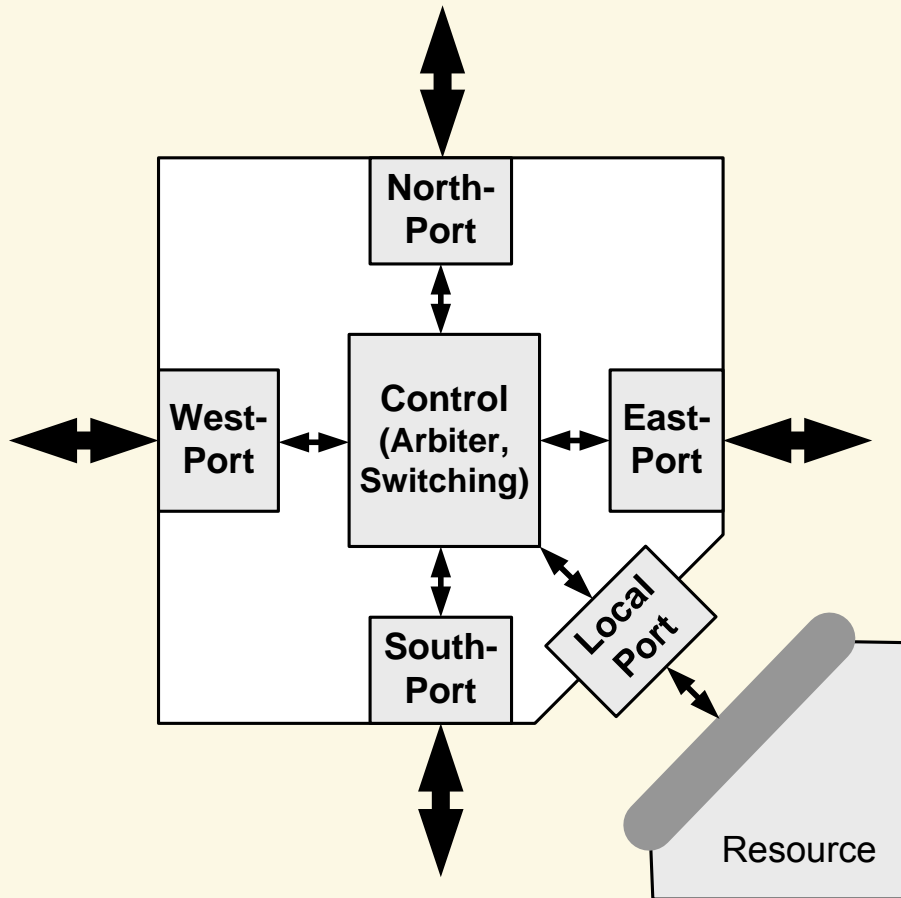
4. Leakage Reduction of NOC Switches



Network-on-Chip

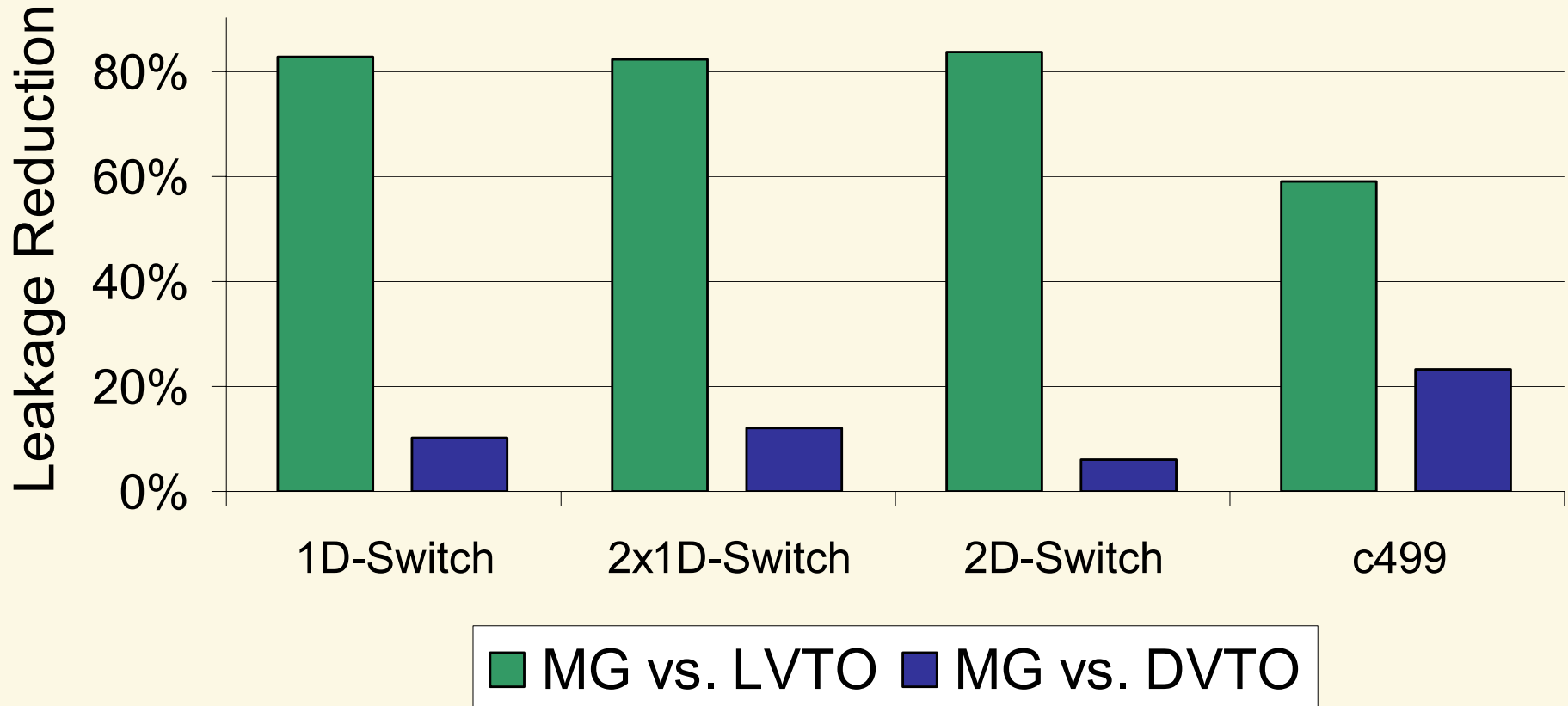


Switch – Architecture



Bus width	16
Gate-Count	1,937
FF-Count	193
Frequency	337.6 MHz
P_{dyn}	214.7 μW

Simulation Results



5. Conclusion

- Subthreshold current and gate oxide leakage dominate leakage power
- *Mixed Gates* approach combines advantages of DVTCMOS and DTOCMOS at transistor and gate level
- Average 83% (vs. *LVTO*) and 10% (vs. *DVTO-CMOS*) leakage reduction at constant delay