Mixed Gates: Leakage Reduction techniques applied to Switches for on-chip Networks

Frank Sill, Claas Cornelius, Stephan Kubisch, Dirk Timmermann
Institute of Applied Microelectronics and Computer Engineering
University of Rostock, Germany
{frank.sill; claas.cornelius; stephan.kubisch; dirk.timmermann}@uni-rostock.de

Abstract

The power dissipation due to leakage currents increases dramatically and endangers various aspects of current and future integrated circuits. However, the issue is recognized and several proposals have already been made to cope with this. Unfortunately, leakage reduction is often traded off for performance. Therefore, an enhanced Dual V_{th} / Dual T_{ox} CMOS approach is presented, which achieves an average leakage reduction of roughly 70 % without any drawback on performance compared to a standard approach. This corresponds to an additional reduction of 20 % compared to a Dual V_{th} / Dual T_{ox} CMOS approach. The paper introduces the used transistor and gate types before a testbench of switches for a network-on-chip and the achieved results are presented and discussed.

1. Introduction

The reduction of power dissipation is a primary concern of current research in the field of integrated circuits. However, the user demand for high mobility and long operation time, especially of battery-operated devices, is contrary to the demand for high performance. Both demands could be satisfied for decades by aggressive downscaling of technology parameters. Thereby, the capacitive load per logic gate could be reduced which has allowed ever higher performance as well as decreased dynamic power consumption. Unfortunately, the influence of short channel and tunneling effects has increased exponentially which has resulted in dramatically increased leakage currents. It is predicted that the power dissipation due leakage currents will be up to 50 % of the overall power consumption [1]. This development paired with the increasing logic complexity of integrated circuits also intensifies power density issues.

The consideration of power savings during idle mode is a very common approach to reduce leakage currents. An example of such an approach is the deployment of so called sleep transistors to disconnect the supply voltage from a design module that is idle [2]. Another attempt, called Minimum Leakage Vector, is to employ special input vectors to the gate inputs [3]. This technique bases on the fact that the leakage of a gate depends on its input vector. Yuan et. al. improved the idea by inserting additional gates [4]. As the supply voltage has significant impact on delay and power consumption, Maken et. al. proposed in [5] to scale the supply voltage according to the required performance.

Another widely used approach is the application of two device types that vary in their threshold voltage V_{th} [6] or gate oxide thickness T_{ox} [7]. Thus, the devices differ in performance and leakage currents. These so called Dual V_{th} CMOS (DVTCMOS) and Dual T_{ox} CMOS (DTOCMOS) design techniques apply fast gates in critical paths and slower gates with lower leakage are used in non-critical paths. Unlike these two approaches on gate level, Wei et. al. [8] present the DVTCMOS approach based on transistor level. That is, single transistors in the design are exchanged by transistors with high V_{th} or low V_{th}, respectively.

The general problems of common leakage reduction techniques are the need of additional devices (e.g. sleep transistors) or that only one component of leakage is reduced. Moreover, transistor level approaches are not applicable for standard cell designs and require long calculation time. Further, gate level DVT- and DTOCMOS methods do not offer the best possible solution because the number of gate types limits the improvement.

Besides the problems of leakage currents, the scaling of technology parameters results in further serious issues that have to be challenged to maintain the performance increase of previous decades. Therefore, interconnects dominating the overall system performance, crosstalk, synchronous clock distribution, reliability, power supply noise, verification, and soft-errors represent just an extract.

Networks-On-Chip (NOCs) have been proposed as a new promising design paradigm to cope with these current issues [9][10]. Figure 1 depicts a simple NOC which consists of miscellaneous independent resources that might work with different voltages, frequencies or even diverse technologies. The resources are connected to a global network by an interface that encapsulates the communication- and computation-structures from another. The network features services such as guarantees for bandwidth or latency that enable the resources to communicate with each other. The network itself consists

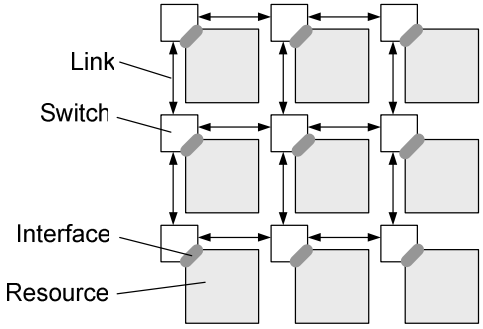

Figure 1. Basic structure of 3x3 Network-on-Chip with a mesh topology

of switches that are connected to each other by physical links. In contrast to bus-based systems, the network is no shared medium so that the switches have to route the data to the correct destination while also considering aspects like congestion or throughput. Therefore, it is apparent that the comprehensive requirements for a switch result in fairly large implementations that consume a significant part of the overall power.

This paper analyzes the implementation of different transistor and gate types, and presents an enhanced DVT-/DTOCMOS approach which is based upon the obtained results for the gate types. The necessary basics are introduced in section 2 before the modified approach is presented in section 3. The used test designs of several NOC switches and the achieved results are described in section 4 before the paper is concluded in section 5.

2. Fundamentals

In the following, a brief description is given to understand the basic idea of the DVT-/DTOCMOS approaches and the correlations of transistor parameters in MOSFET technologies with gate length below 100 nm.

2.1. Delay

The delay of CMOS can be approximated as:

$$delay \quad \frac{C_{load} V_{DD}}{m\,(e_{ox} / T_{ox})\;(W_{eff} / L_{eff})\,(V_{DD} - V_{th})^{a}}$$

C_{load} denotes the gate's load capacitance, V_{DD} is the supply voltage, μ and ε_{ox} correspond to the physical constants electron surface mobility and gate oxide's dielectric constant, W_{eff} and L_{eff} are the effective gate width and length, respectively, V_{th} is the threshold voltage, and α is the velocity saturation index [11]. Further, V_{th}, which has a strong impact on delay, can be modeled as [12]:

$$V_{th} = V_{th0} + g'\sqrt{NDEP}\;\; T_{ox} V_{bs} - h' \frac{T_{ox}}{L_{eff}^2\;\sqrt{NDEP}} V_{ds}$$

V_{th0} is the zero-bias threshold voltage, V_{bs} is the bulk-source voltage, V_{ds} is the drain-source voltage, γ' is the body-bias coefficient, η' is the drain induced barrier lowering (DIBL) coefficient, and *NDEP* denotes the channel doping concentration. It can be observed from this equation that the process parameters T_{ox} and *NDEP* influence the threshold voltage V_{th} the most.

2.2. Dynamic power dissipation

To process data in an integrated circuit, parasitic capacitances caused by logic gates and interconnects have to be charged and discharged, respectively. This results in the so called dynamic power dissipation P_{dyn} which is given as:

$$P_{dyn} = p_{0\text{fi}1}\;\; f\;\; V_{DD}^2\;\; C_{load}$$

$$C_{load} = \sum_{transistors} C_{in} + C_{wire}$$

$$C_{in} \gg W_{eff}\;\; \frac{e_{ox}\;\; L_{eff}}{T_{ox}}$$

$p_{0\rightarrow1}$ denotes the probability for a low-to-high transition of the gate's output, f is the design frequency, and C_{load} is the capacity of the gate output and can be calculated as the sum of all connected input capacitances C_{in} plus the wire capacitance C_{wire}.

2.3. Leakage

Ideally, CMOS gates draw no current or rather dissipate no power when idle. Unfortunately, this is not true for real gates. The strongest impact originates from the sub-threshold current I_{sub} and the gate oxide current I_{gate}. The former is the current between source and drain of a transistor when the device should in fact be cut off ($V_{gs} < V_{th}$). A commonly used approximation of the sub-threshold current I_{sub} is [12]:

$$I_{sub} = I_0\;\; \frac{\sqrt{NDEP}}{L_{eff}}\;\; e^{\left(\frac{q}{nkT}(V_{gs} - V_{th})\right)}\;\; \left|1 - e^{\left(-\frac{kT}{q}V_{ds}\right)}\right|$$

Here, I_0 is the zero-bias current, T is the operating temperature, n is the sub-threshold swing coefficient, V_{gs} is the gate-source voltage, k is Boltzmann's constant, and q corresponds to the charge of an electron. Following from this, I_{sub} highly depends on V_{th}, which is most sensitive to the technology parameters T_{ox} and *NDEP*.

The second important contributor of leakage currents is the gate oxide current I_{gate} which bases primarily on tunneling currents through the gate's dielectric. Physically, these are the direct tunneling (DT) current in the gate-channel region, and the edge direct tunneling current (EDT) in gate-drain/gate-source overlapping regions. The current density for both direct tunneling currents can be described as [13]:

$$J_{DT} = A \left(\frac{V_{ox}}{T_{ox}}\right)^2 exp\left(-B\left[1 - \left(1 - \frac{V_{ox}}{\Phi_{ox}}\right)^{3/2}\right] \frac{T_{ox}}{V_{ox}}\right)$$

V_{ox} is the potential drop across the gate oxide, Φ_{ox} is the barrier height for the tunneling particle (electron or hole), and A and B are physical parameters. In contrast to sub-threshold current, gate oxide current is most sensitive to T_{ox} only.

2.4. Dual Vth / Dual Tox CMOS

Data signals traverse integrated circuits through different paths of logic gates whereas the start- and endpoints of these paths are marked by sequential elements like registers. The maximum frequency to clock the registers is determined by the path with the longest propagation delay, called critical path. Thus, it is possible to trade off delay for leakage in all other, non-critical paths. Such an attempt is exploited by the Dual V_{th} CMOS (DVTCMOS) und Dual T_{ox} CMOS (DTOCMOS) techniques. Therefore, both approaches offer various gates for the same logical function that differ in evaluation delay and power dissipation due to leakage currents.

As shown in the previous sections and in [14] and [15], the transistor's threshold voltage V_{th} and thickness of the gate oxide layer T_{ox} mainly determine delay and leakage. So, DVT- and DTOCMOS approaches apply fast gates with transistors that have low V_{th} (LVT gates) or low T_{ox} (LTO gates), respectively. Further gates are used that have the same logical functions but consist of transistors with high V_{th} (HVT gates) or high T_{ox} (HTO gates). These gates offer slower evaluation but also decreased leakage currents. Finally, to reduce the design's overall leakage currents at constant performance, as many HVT or HTO gates as possible are applied to the non-critical paths so that the delay of the paths does not exceed the critical path delay which consists solely of LVT or LTO gates [6][7]. In the following, the combination of DVTCMOS and DTOCMOS is called DVTO. Hence, DVTO approaches apply transistors with different T_{ox} and V_{th}.

3. Mixed Gates

This section describes the fundamental idea of *Mixed Gates* and how the different transistor and gate types were derived. Finally, the creation of a gate library and how to allocate the different gate types in a design is presented.

3.1. Fundamental idea

The idea of the *Mixed Gates* design technique is the combination of advantages from gate level and transistor level approaches. That is, high accuracy and applicability for a standard cell design flow. In addition, the *Mixed Gates* approach merges the technological attempts of DVTO approaches.

As shown in section 2, in [14], and [15], the transistor's leakage as well as the delay highly depends on V_{th}, T_{ox}, and *NDEP*. Against this background, it was sought after new transistor types. Transistor models of a predictive 65 nm technology were used as base technology [14][16] and as a result of extensive simulations, two types of transistors were defined. The first type of fast switching transistors *L-Vt/To* with high leakage currents, has low T_{ox} and low *NDEP*, which results in low V_{th} and short delay. The second transistor type *H-Vt/To* has high T_{ox} and high *NDEP*, which results in high V_{th}. The latter transistors switch slower but have lower gate oxide leakage as well as reduced sub-threshold leakage. With the modified transistor types, HVTO gates consisting solely of *H-Vt/To* transistors and LVTO gates consisting solely of *L-Vt/To* transistors, could be implemented (see figure 2). At this stage, leakage reduction based on the idea of DVTO approaches can be performed.

However, the *Mixed Gates* approach offers two additional gate types which are called standard Mixed Gates (MG) and Fast Mixed Gates (F-MG). F-MG gates contain few *H-Vt/To* transistors at adequate positions, so that the delay is equal to corresponding LVTO gates but the leakage is lower. Therefore, LVTO gates are not used any further because they can be replaced by F-MG gates without any drawback on performance due to the equal delay but lower leakage. Finally, MG gates contain mainly *H-Vt/To* transistors, so that the gate delay is in between the delay of F-MG and HVTO gates. Figure 2 depicts the different introduced implementations of a NOR2 gate and table 2 classifies the used mixed gate types qualitatively.

When applying the *Mixed Gates* approach, a design is initially implemented with only F-MG gates. Then, as many gates as possible are exchanged by appropriate MG and HVTO gates so that the maximum delay is not

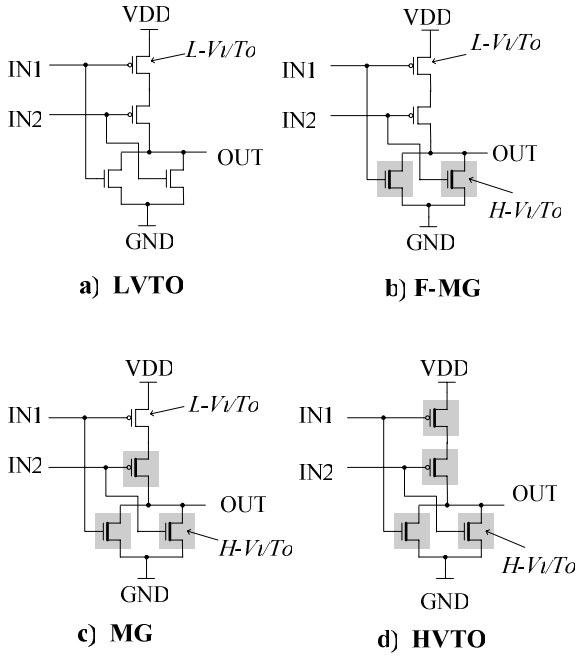

Figure 2. Different implementations of a NOR2 gate: LVTO, HVTO, and Mixed Gates

Table 1. Classification of gate types that are applied by the Mixed Gates design technique

	HVTO	MG	F-MG
Delay	High	Medium	Low
Leakage	Low	Medium	High
Applied transistor types	H-Vt/To	H-Vt/To and few L-Vt/To	L-Vt/To and few H-Vt/To

increased. That is, the critical paths consist solely of F-MG gates whereas all other paths apply a combination of the three gate types so that the path delays do not exceed the critical path delay. Thus, the *Mixed Gates* approach offers three advantages:

- larger amount of low leakage devices within a design as in DVTO approaches
- reduction of both main sources of leakage currents: the gate oxide leakage I_{gate} and the sub-threshold leakage I_{sub}
- no drawback on performance compared to the original designs, which consist of fast and high leakage devices

3.2. Different Gate Configurations

The implementation of a *Mixed Gates* library requires design rules for the positioning of different transistor types. These rules ease the design of new MG and F-MG gates so that for instance not all possible input combinations need to be tested. The extracted rules are:

Delay rule: *Within mixed stacks, the L-Vt/To transistors have to be placed as close as possible to the gate output to achieve best results for the delay.*

Leakage rule: *Within mixed stacks, the H-Vt/To transistors have to be placed at the end of the stack (away from the output) to achieve best leakage results.*

Fortunately, both rules lead to the same configurations. While the delay rule has significant influence on the gate's properties, the leakage rule leads only to slightly different results. Further, it can be observed that the F-MG gates with deep NMOS stacks, i.e. large number of sequential NMOS transistors, should be built with mixed transistors. In contrast, F-MG gates with PMOS stacks should not be built with mixed transistors, rather with parallel *H-Vt/To* NMOS transistors. However, this behavior cannot be formulated as a rule, because it depends on the relationship between PMOS and NMOS transistors of the applied technology. Hence, the described recommendations can be an entry-point but the different cases have to be investigated thoroughly to achieve optimal results.

3.3. Library Creation

Based on the mentioned rules, a gate library with 10 standard gates was implemented. This comprised the sizing of each gate, which means adjustment of the effective gate width W_{eff} for every single transistor. In contrast to T_{ox} and *NDEP*, W_{eff} is a design parameter, which is not fixed within a technology and can be modified by the library designers. It was shown in section 2 that an increasing W_{eff} results in decreased gate delay, but increased dynamic power dissipation. Thus, the goal for the sizing should be the smallest possible W_{eff} for every transistor so that the delay still achieves the desired value. The sizing was performed with the Cadence® Analog Circuit Optimizer. Table 2 displays the applied options for the optimizer.

Further, for some gates all possible transistor type combinations were implemented to verify the presented rules. Figure 3 and figure 4 depict some of the results for NAND3 and NOR3 gates. The data points' second triple of letters indicates the types of PMOS transistors and the last triple indicates the types of NMOS transistors. Thereby, 'H' denotes *H-Vt/To* transistors, while 'L' denotes the *L-Vt/To* ones. The underlined configurations were finally chosen for the gate library.

Table 2. Options of the different gate types for the circuit optimizer

LVTO	- each input has the same C_{in} - balanced maximum delays for the falling and rising slopes (± 10 %)
HVTO	- same C_{in} for each input as the corresponding LVTO type - same C_{in} of internal inverters as in AND / OR gates - balanced maximum delays for the falling and rising slopes (± 10 %)
MG	- same C_{in} for each input as the corresponding LVTO type - same C_{in} of internal inverters as in AND / OR gates - balanced maximum delays for the falling and rising slopes (± 10 %)
F-MG	- about the same sum of C_{in} (including internal loads) as the corresponding LVTO type (± 10 %) - about the same C_{in} for each gate input as in the corresponding LVTO type (± 10 %) - same maximum delay as the corresponding LVTO type - balanced maximum delays for the falling and rising slopes (± 10 %)

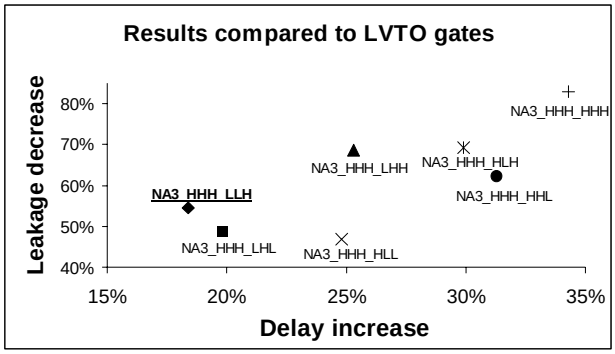

Figure 3. Comparison of possible MG realizations for a NAND3 (NA3) gate

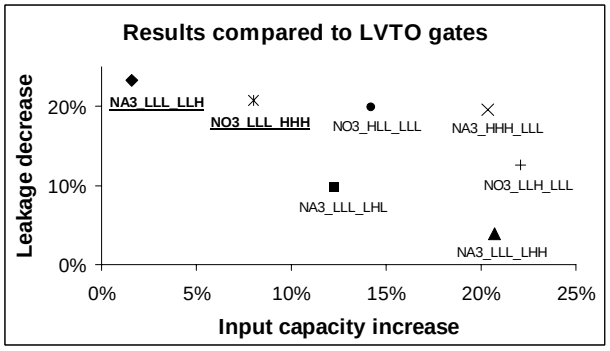

Figure 4. Different implementations of F-MG for a 3-input NAND (NA3) and NOR (NO3) gate

The properties of the chosen gates indicate that compared to LVTO gates the input capacitance of the chosen F-MG gates increased by in average 3 %, the leakage decreased by 20 %, and the delay remained constant. Further, the chosen MG gates offer medium delay compared to corresponding HVTO and LVTO gates, while the leakage could be decreased by over 50 % compared to LVTO gates and the input capacitance stayed constant.

3.4. Gate Type Allocation Algorithm

An allocation algorithm is needed to apply the different gate types at appropriate positions so that the leakage is reduced without influencing the system delay. The developed algorithm bases on weighting of each gate of the design [17]. The weight factor of each gate is calculated from its leakage, delay, and slack. The latter is the time by which a gate can be slowed down without influencing the design performance. In the initialization phase, each gate is set to the F-MG type. Based on the weight, MG gates or a HVTO gates are applied if possible.

It follows a pin reordering to consider dependency of gate leakage on the input values. The interested reader is referred to [7][17] for a detailed description of the pin reordering and the applied algorithm.

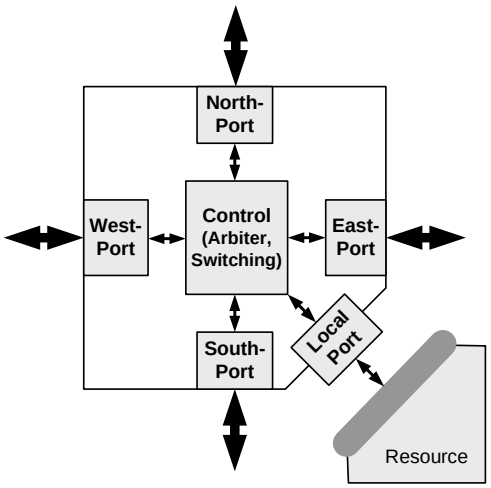

Figure 5. Basic structure of a 2D switch with five ports for dimension-ordered routing

4. Simulation and analysis of NOC-switches

Up to date, a large number of solutions for the implementation of NOC switches have been presented [18][19]. The various designs can be distinguished by for instance speed, buffering, routing scheme, arbitration, switching, and number of ports. However, the main focus has been put on functionality and flexibility whereas only few attempts have been made to reduce the power consumption caused by leakage currents. Therefore, to employ the *Mixed Gates* technique on NOC switches can not only proof the effectiveness of the approach but also provides a gain in knowledge for the power characteristics of the switches.

4.1. Design of the NOC-Switches

The emphasis of this paper is not on the design or the functionality of the NOC switch but on the *Mixed Gates* approach. Hence, this section covers only briefly the concept and design of the switch. The interested reader is referred to [20] for a more detailed description.

The main task of the implemented switches is dimension-ordered routing with absolute addressing. XY-routing is such an example where data are routed horizontally first until they reach the final column. Then, the data are routed vertically to the destination. Several subtasks are needed to perform the routing. At the ports, flow control is required to interrupt transmissions in case that no more incoming data can be processed. The arbiter decides and allocates the output ports when a single link is requested several times concurrently. Finally, the physical switching has to be performed to direct the data to the appropriate output. Figure 5 depicts the basic structure of a 2-dimensional (2D) switch where all ports are connected to other switches except for the local port being connected to the local resource.

Three different versions of the switch were implemented with a bus width of 16 bit. The first switch supports only 1-dimensional (1D-switch) routing and offers three ports. That is, switches can only be aligned sequentially in a line or a circle, respectively. The second

Table 3. Simulation results for the three switches and a reference design from the ISCAS'85 test suite [21]

		1D-Switch	2x1D-Switch	2D-Switch	c499
Gate-Count		824	1,764	1,937	474
FF-Count		105	214	193	0
Frequency		1,082.3 MHz	483.0 MHz	337.6 MHz	742.9 MHz
Leakage currents	LVTO	103.5 µA	215.7 µA	234.2 µA	76.2 µA
	DVTO	19.9 µA	38.2 µA	47.1 µA	40.9 µA
	Mixed Gates	17.9 µA	35.9 µA	41.4 µA	31.4 µA
Total PDP	LVTO	425.3 fJ	1,019.1 fJ	1,260.3 fJ	482.7 fJ
	DVTO	355.8 fJ	759.1 fJ	761.5 fJ	439.9 fJ
	Mixed Gates	354.1 fJ	754.8 fJ	746.3 fJ	428.3 fJ

switch is derived from two 1D-switches (2x1D-switch) whereas the last switch is a straight on implementation of a 2-dimensional switch (2D-switch). This means that the latter two versions could be used for the implementation of a mesh network, as shown in figure 1.

4.2. Simulations

The three switch designs were analyzed as well as the design c499 from the ISCAS'85 test suite to have a comparison with well known results [15][17][21]. Therefore, all designs were synthesized using the developed *Mixed Gates* library as well as the LVTO and the DVTO library to compare the achieved results among each other. To clarify this, the LVTO version of each design consists solely of LVTO gates whereas the DVTO version is based on traditional DVTCMOS and DTOCMOS approaches. Hence, these design versions apply HVTO and LVTO gates. Thereby, the gate allocation algorithm was the same for all designs and approaches (see section 3.4).

After the final netlists were generated, the analysis of each design version followed, that is, to determine the maximum frequency f_{max}, the leakage currents, the dynamic power dissipation P_{dyn}, and the power-delay-product PDP. The determination of P_{dyn} was based on the transport of originally random payloads applied to the ports. However, the generated data pattern was then equal for all designs. Finally, P_{dyn} was measured with the Synopsys PowerAnalyzer® at the maximum design frequency. The leakage currents were determined with HSpice® for an input probability of 0.5. As the sequential elements like registers were not changed by any of the applied approaches, these elements were ignored during the analysis of the results.

4.3. Results

The results of the simulations are depicted in figure 6 and table 3. Foremost, it was observed that all designs work with the same frequency, which proves that leakage reduction was not traded off for performance. However, there were major differences for the appearing leakage. As expected, the LVTO designs have highest leakage currents. Within the switch designs, the *Mixed Gates* approach could reduce the leakage by an average of 83 %. This is an additional improvement of approximately 10 % compared to the DVTO designs. The tendency is similar for the c499 design where the *Mixed Gates* approach reduces leakage by 58 % compared to the LVTO version and by 23 % compared to the DVTO version. Nonetheless, the difference of improvement between the switches and the c499 design is clearly observable which can be explained by looking at the design structures. The switches are implemented in two pipeline stages whereas the second stage has a much shorter critical path compared to the first stage. As the design frequency depends only on the slowest overall path, the second stage

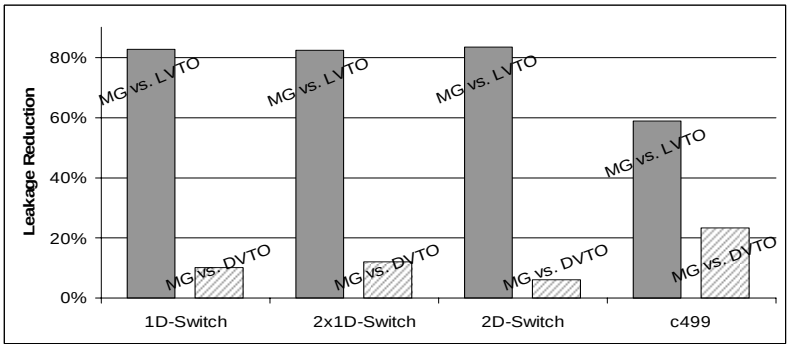

Figure 6. Achieved reduction of leakage currents for the Mixed Gates approach compared to LVTO and DVTO designs

Table 4: Leakage Reduction of Mixed Gate versus DVTO designs for each pipeline stage

	1D-Switch	2*1D-Switch	2D-Switch	c499
1st stage	11.94%	7.22%	15.23%	23.36%
2nd stage	3.61%	0.00%	0.00%	-
Overall	10.23%	6.00%	12.10%	23.36%

can almost completely be implemented using HVTO gates. Hence, the *Mixed Gates* approach cannot exploit its advantages, which reduces the overall reduction compared to DVTO designs. Table 4 summarizes the results for the two pipeline stages whereas it can be seen that no further improvement was achieved in the 2nd stage of the two-dimensional switches.

The dynamic power dissipation P_{dyn} of the implemented switches is relatively small due to the low activity within the switches. Besides, P_{dyn} is roughly equal above all designs so that a detailed discussion is not carried out.

5. Conclusions

The modification of transistor parameters and their impact on delay and power was presented. Based on the achieved results, four different gate types were derived that differ in delay and leakage but perform the same logical function. Then, the *Mixed Gates* design technique was applied to several versions of a NOC switch and the results were evaluated. Concluding, the proposed *Mixed Gates* design technique works successfully and can reduce leakage currents without any drawback on performance by as much as 83 % compared to a standard approach. Moreover, the results of common DVTO approaches were further improved by about 10 %. Hence, the *Mixed Gates* approach is a promising option to reduce leakage currents, not just in NOCs but in designs of any kind.

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