Norchip

THE NORDIC EVENT IN ASIC DESIGN

Total Leakage Reduction by Observance of Parameter Variations

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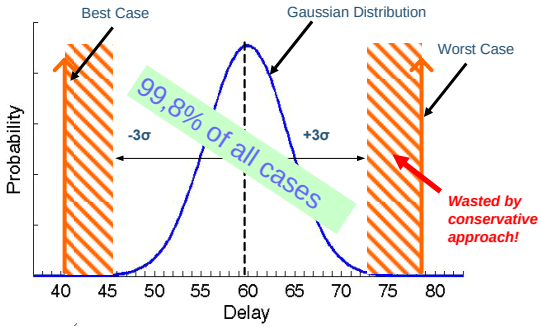
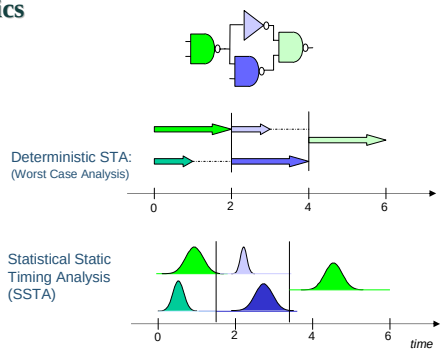
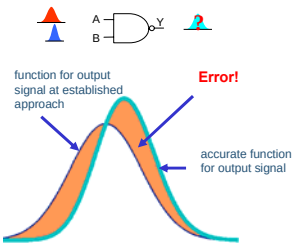
Statistical STA Basics



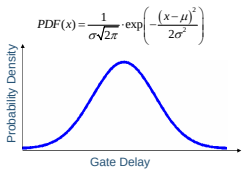


New Approaches for Delay Modeling and SSTA at MIS Gates



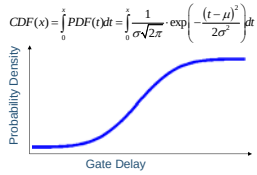
Probability Density Function (PDF)

Probability that gate delay has value x



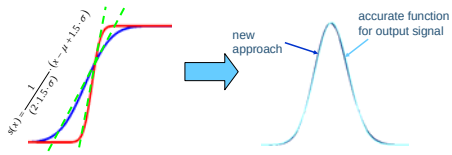
Cumulative probability Distribution Function (CDF)

Probability that gate delay is lower than x



New Approach for SSTA on Multi-Input Gates:

As function of output signal results from multiplication of all input CDFs
CDF is approximated as straight line
=> new CDF results from multiplication of all approximated straight lines of input signals

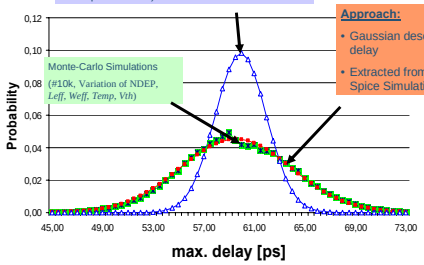


Evaluated delay if only less parameters are described with Gaussian distribution

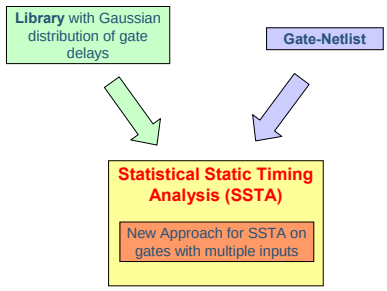
(usually used, because high effort to describe more parameters)

Approach:

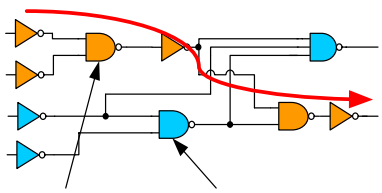
- Gaussian description of gate delay
- Extracted from Monte-Carlo Spice Simulation



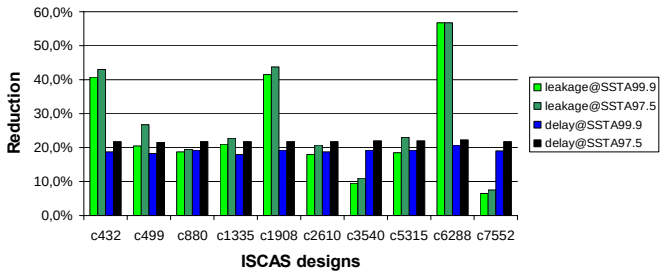
NAND2 in predictive 65nm BPTM technology



Dual Vt/To CMOS and Results



Leakage or Delay Reduction by SSTA @ preoptimized Dual Vt/To CMOS circuits



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