Temperature and On-chip Crosstalk Measurement using Ring Oscillators in FPGA

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***Abstract*—Temperature management and signal integrity are two highly relevant challenges for nano scale CMOS devices. As temperature of integrated circuits affects the frequency of defect mechanisms' occurrence and consequently influences reliability, temperature monitoring is inevitable. To provide the necessary thermal sensors, different techniques are available. One is to use the temperature dependent speed of logic devices and perform a time to digital conversion. In this work, this approach is evaluated for the use in FPGAs. Furthermore, problems regarding signal integrity affect the reliability of highly integrated circuits. Therefore, we discuss the possibilities of crosstalk effects in FPGA and demonstrate a method for time to digital conversion in order to measure the impact of coupling capacitances in the interconnection structure of FPGAs. The main contribution of the introduced method is to enable simple post-production investigations for signal integrity of programmable devices.**

I. Introduction

The increasing integration density of CMOS technology introduces problems concerning growing power densities. Although the power dissipation has slightly been reduced, local power density of systems in an active state grows enormously. This leads to higher temperature densities of chips and adds problems like thermal imbalances and hotspots.

Especially process variations - inter and intra die - are leading to different threshold voltages of the devices. This entails dynamic power and leakage variations on a chip and between different chips of the same type. In multi-purpose many core systems like Systems-on-Chip the load-idle balance of the system is considered to be one critical issue. The resulting thermal imbalances and hot spots may be difficult to detect from the perspective of system management. Dynamic thermal monitoring and management are feasible solutions, sensing temperatures in a distributed manner at different positions on the chip.

Another issue of current chip design is signal integrity. Due to process variations and temperature drift the characteristics of signals simulated during preproduction can significantly change. A special phenomenon affecting signal integrity is on-chip crosstalk induced by coupling capacitances between large nets. Unfortunately, it is difficult to measure how much influence crosstalk actually has on the signals. In most cases pessimistic pre-production simulations must be sufficient. Additionally there are parameter tests of MOS devices (PATMOS) for every new process-iteration or every run. Furthermore the interconnection and routing resources are not as fast growing as the functional ones. All this also applies to programmable devices and makes e.g. field programmable gate arrays (FPGAs) prone to signal integrity issues like crosstalk. In case of programmable logic devices a special configuration implementing a measurement circuit can be used for post-production measurements.

In this work we show, that well known circuits for measuring temperature in digital CMOS devices can easily be used on FPGAs. However, the main contribution is the demonstrated measurement of crosstalk induced delay with a similar method. The proposed technique can also be used for academic purposes to make temperature and crosstalk visible as intrinsic analog effects by the use of digital circuits.

II. Related Work

Most methods to measure temperature in integrated systems are leading back to thermoelectric effects known as Peltier, Seebeck or Thomson effect. Another possibility is using the junction forward voltage of a diode and feeding the resulting voltage with respect to a known reference to an analog digital conversion (ADC) [1]. A third possible method is using the temperature dependent behavior over time of digital circuit elements. This is also based on the temperature dependence of the junction voltage and the temperature dependent mobility of electrons and holes. In this case the ADC is transformed to the concept of time to digital conversion.

Utilizing ring oscillators as temperature sensors is quite common. In the field of FPGAs e.g. Boemo and Lopez-Buedo [2], [3] used features like dynamic reconfiguration to implement the oscillator. They implemented three inverters packed into two configurable logic blocks (CLB) to only use minimal area. The error was maintained near 1 °C. Furthermore, they recognized that changes to the supply voltage had an influence on the measured frequency of the oscillator.

Velusamy et al. [4] used the technique for dynamic temperature measurement in FPGAs and checked with the thermal simulation framework HOTSPOT [5]. A multi sensor array for FPGAs was proposed by Zick et al. [6] including a very small implementation of a ring oscillator and a frequency counter.

The digital delay measurement of crosstalk effects was proposed by Su et al. [7]. The delay was captured with a phase difference counter in this work. A ring oscillator and a frequency counter were used by Tanaka et al. [8]. They produced a test chip to make the influence of crosstalk visible.

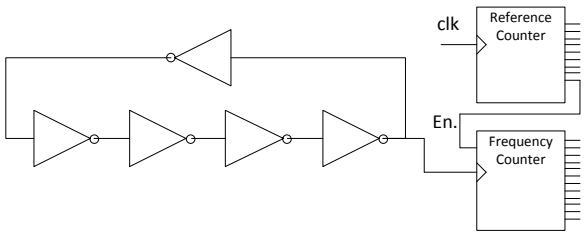

Fig. 1. Schematic of a ring oscillator and frequency counter, which is enabled by a reference counter

In this work we will show that on-chip crosstalk is even measureable on FPGAs. We will show a simple way of making the two different analog phenomena temperature change and crosstalk effect visible using digital devices.

III. Ring Oscillators in FPGAs

In FPGAs logic functions are implemented in configurable logic blocks (CLB). They contain lookup tables (LUT) and registers. The delay of a LUT is independent from the eventually configured Boolean function. The CLBs are connected with switch matrices. Two or more switch matrices are used to build a path from one CLB to another, this is called routing.

A ring oscillator is a circuit that is oscillating because of its inherent logic function. It can be implemented by the use of an odd number of digital circuit elements that realize an inverting function. For a FPGA this means that LUTs are configured as inverters and a chain of LUTs is building the oscillation loop.

A simple way to measure the frequency of the oscillator with purely digital elements is to use two counters. One of them is generating a defined span of time with the help of a known clock rate. This reference time is used to enable the second counter which is counting the slopes in the ring oscillator (see fig. 1).

If one or more of the delays are changing, a frequency drift of the ring oscillator can be observed. Most of the influences on delay are leading back to changes of temperature and variations of supply voltage. Another reason for delay fluctuations are found in neighboring circuit elements causing crosstalk effects.

A. Temperature

The temperature of the circuit influences the oscillation speed of a ring oscillator via different parameters. On the one hand, the threshold voltage of CMOS devices is decreasing by 2 to 4 mV per Kelvin (see eq. 1) [9]. The exact figures depend on the doping level of the actual semiconductor. This change of threshold voltage is leading to higher drain currents at increasing temperatures. The circuit is getting faster.

$$Vt = Vt_0 + \alpha_{Vt} \cdot (T - T_0) \quad \text{for } \alpha_{Vt} = -2 \ldots -4 \left[\frac{mV}{K}\right] \tag{1}$$

$$\mu = \mu_0 \cdot \left(\frac{T}{T_0}\right)^{\alpha_\mu} \quad \text{for } \alpha_\mu = -1.5 \ldots -2.5 \tag{2}$$

TABLE I
Crosstalk patterns with switching example

pattern name	switching example
0C	$000 \rightarrow 111$
1C	$000 \rightarrow 011$
2C	$101 \rightarrow 111$
3C	$100 \rightarrow 010$
4C	$101 \rightarrow 010$

On the other hand, the carrier mobility (μ) in silicon is depending on temperature, too. There are two effects that influence the mobility, lattice scattering and impurity scattering. At normal device temperature ranges like -55 to 125 °C (military grade) the lattice scattering effect will dominate. These value for α_μ depends on doping and varies from -1.5 to -2.5 in literature. This correlation leads to a decreasing drain current. The device is getting slower as the temperature is increasing.

The threshold voltage effect strongly depends on the voltages of the device - mainly drain-source voltage. If the supply voltage is close to the threshold voltage the temperature effect on the threshold voltage is dominating. The dependence between device speed and temperature turns into a positive correlation, this is called the reverse temperature dependence. There is even a point where the mobility and threshold voltage effect are compensating each other [10].

As the temperature coefficient of connection wires is negligible (Cu: 0.0039/K) and with the assumption that the supply voltage is not very close to the threshold voltage, a negative linear correlation between temperature and device speed can be assumed. The circuit (see fig. 1) was extended to be able to control the time the loop is oscillating and the time the counter is running. Additionally, a possibility to choose between four different lengths of the oscillation loop was designed.

A potential error source for the accuracy of the measurement is the self-heating of the circuit induced by switching activity. To minimize this effect we make the measurement cycle short and deactivate the oscillation when no measurement is needed. A further error source would be a variation of the supply voltage.

B. Crosstalk

Crosstalk is the inductive and capacitive coupling between two or more nets. Inductive crosstalk is an issue at very high frequencies that will not be reached on today's FPGA devices. Hence, we are concentrating on capacitive crosstalk effects. A net provides capacitances to ground and the neighboring nets. An observed net is considered as the victim and its neighbors are aggressors. If the voltage level on the aggressors is changing, a change of the effective coupling capacitance can be observed. The effective coupling capacitance can increase or decrease depending on wether the aggressor transmits the same or the oposing slope. How much the delay is changing depends on the ratio of ground and coupling capacitance. Five patterns of these changes can be identified (see table I). These can result in glitches, delay increases or delay decreases which lead to errors if timing margins are not sufficient.

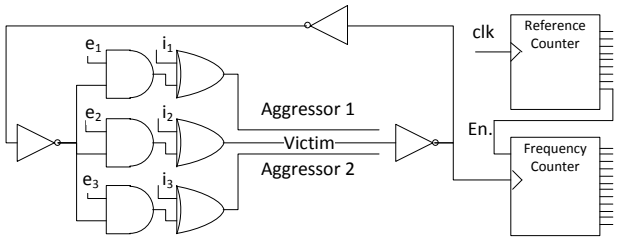

Fig. 2. Schematic of a measurement circuit for crosstalk induced delay

For the measurement of changes in crosstalk induced delay a similar circuit as the temperature sensor can be used. The ring oscillator is designed to contain a test line that is used as the victim net (see fig. 2). To create synchronous aggressors this wire is tripled. As there are different crosstalk patterns to create, XOR and AND gates are inserted. In this way the voltage level on the aggressors can be inverted in respect to the victim or the aggressor can be made static. Now, all patterns can be created by choosing the right inputs for the XOR and AND gates.

IV. Implementation

For the implementation of the two measurement circuits containing ring oscillators we used VHDL as the description language. To prevent the synthesis tool from optimizing and deleting the inverter chain, a keep attribute was used. For implementation we used the Xilinx tool environment and the development boards ML507 and ML605 as target platforms providing Virtex 5 and Virtex 6 FPGA devices. These devices are produced at 65 respective 40 nm technology nodes by UMC and Toshiba.

To get maximum control over synthesis, routing and placement processes user constraints were applied in order to limit the possible implementation options of the used design automation tools. To place the ring oscillator at a specific position on the FPGA, location constraints where used to define the positions of the LUTs the inverters are implemented in. For the crosstalk measurement it was essential to route the aggressors as actual neighbors to the victim net on the whole path. For this task manual routing and directed routing constraints were used.

The switch matrices of the used FPGA are connected utilizing different routing channel types. Signals can be routed through these links that differ in the distance they bypass in horizontal, vertical or both directions. For Virtex 5 generation FPGAs there are Double, Pent, Long and Global links, bypassing a different number of switch matrices (2, 5, 18, 19). Where Virtex 6 devices use Double, Quad, Long and Global links (2, 4, 16, 19). To get a set of different lengths we combined multiple (1, 2, 3 and 4) of the Long links.

To get the measured frequency in machine readable format out of the FPGA and control the measurement process we used the on-chip processor provided by Virtex 5 and a soft-core processor in Virtex 6. The counter register was connected to a communication bus. In that way it could be read and a configuration register could be written by the processor.

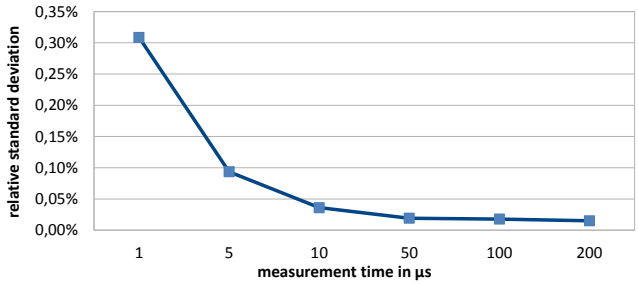

Fig. 3. Relative standard deviation of frequency measurements at a specific temperature over different time spans of measurement

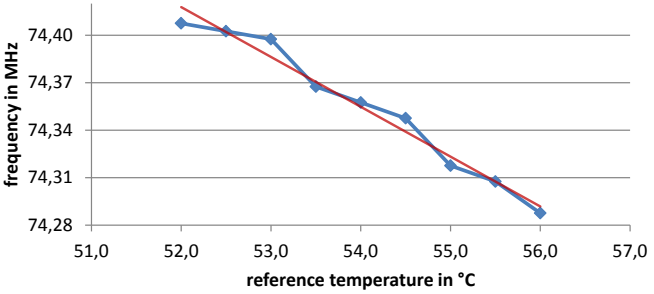

Fig. 4. Linear relationship between temperature and oscillation frequency

V. Results

A. Temperature

The temperature measurement was validated with the help of an on-chip temperature sensor provided by the FPGA. It is implemented using a dedicated diode at the center of the die [6]. Its uncertainty is $\pm 4\,^{\circ}\mathrm{C}$. So the implemented sensor was placed close to the center of the FPGA as well.

The implementation of different rings in terms of the number of inverters allows an investigation of the precision reached by different implementations. The used ring sizes were 5, 8, 13 and 22 LUT delays. Further, different time spans for warm up and measurement were used. The measurement time was varied from 1 to 200 µs (see fig. 3), the warm up time between 0 and 200 µs. For each parameter variation we averaged 10,000 measurements and compared the standard deviation as a measure of precision. As the longest ring oscillator and measuring for 200 µs showed the lowest random error of only 0.012 % we chose this parameter set for further measurements. The length of warm up time showed no influence on the precision. Figure 4 shows the linear relationship of 31.7 kHz per Kelvin between frequency and temperature.

As only one way of measuring the temperature is available through the on-chip diode / ADC combination (accuracy $\pm 4\,^{\circ}\mathrm{C}$) this has to be used for calibration. We assume this as the absolute error of the measurements. As it is assumed that the absolute error is constant the random error determined as $0.3\,^{\circ}\mathrm{C}$ defines the accuracy for temperature changes.

An interesting point in using a configurable chip with the possibility to measure the temperature wherever you want, is to provide an array of sensors to compile a temperature map of the device. Even if the relative placement of the ring and the routing between the ring elements is constrained, the

TABLE II
FREQUENCY UNDER INFLUENCE OF DIFFERENT CROSSTALK PATTERNS FOR DIFFERENT LENGTHS IN MHZ (1 TO 4 TIMES ONE LONG LINK)

aggressor length		0C	1C	2C	3C	4C
Virtex 5:	1x	94,3	94,2	93,9	93,3	93,1
	2x	95,0	94,8	94,6	94,0	93,8
	3x	91,7	90,8	90,1	88,7	87,6
	4x	98,4	96,9	95,5	93,4	91,9
Virtex 6:	1x	142,6	141,5	140,2	139,0	137,7
	2x	145,2	143,0	140,6	138,4	136,5
	3x	150,8	147,7	144,2	141,2	138,6
	4x	144,4	141,1	137,4	134,3	131,7

various instances show different frequencies, which can not be explained just by temperature variation. Because of such supply voltage and device variations each sensor would have to be calibrated.

B. Crosstalk

The crosstalk induced delay was measured with the described circuit implementation. A relationship between the configured crosstalk pattern and the oscillation frequency is measureable, if long links are used in the FPGA interconnection fabric. For other link types the correlation was not significant. The physical implementation appears to differ between those link types, e.g. bigger spacing or shielding.

To minimize the error due to temperature drift during the delay measurement, all crosstalk patterns were configured in sequence with minimal time spacing.

The results (see table II) show delay variations for the different aggressor length used. The maximum frequency variation for Virtex 6 amounts from 131.7 to 144.4 MHz for worst respective best case crosstalk patterns. This corresponds to a delay change of 672 ps. For Virtex 5 its 91.9 to 98.4 MHz, which are 719 ps.

A comparison of the two tested devices indicates that the crosstalk influence is more dominant in the Virtex 5, which can be explained by the longer link length. Furthermore, the Virtex 5 device is produced in 65 nm technology while the Virtex 6 is a 40 nm device. The smaller structures on the chip are implying a further decreased interconnection length.

The relative change of delay (normalized to crosstalk pattern 2C, see fig. 5) is indicating how much the delay of the victim line varies through the cross coupling capacitances. The crosstalk induced delay is showing a linear dependency on the length of the aggressor. Furthermore, the delay depends on the crosstalk pattern. The 5 patterns build linear influence where the 0C pattern has the most positive and 4C the most negative effect. The comparison shows that the absolute influence on the delay in Virtex 5 devices is bigger, but as there are higher frequencies possible in Virtex 6, crosstalk is becoming a critical issue to this platform first.

As there are no reference measurements possible for crosstalk induced delay and the post layout simulation data is not available, there is no way of validation and not much to state about precision and accuracy of the measurement. However,

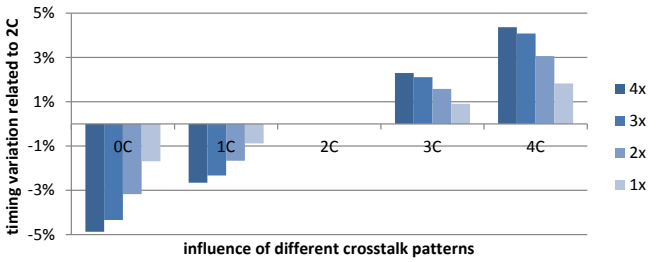

Fig. 5. Crosstalk induced delay for Virtex 6 normalized to pattern 2C

the random error of 10,000 measurements was only 0.0001 % under influence of temperature drift.

In the end it has to be remarked that everything was done without knowing the exact physical implementation and technology data, so we cannot confirm for sure the quantity of the measured results. However, the quality of the gathered results is matching the theory and is showing that crosstalk can influence the signal integrity in FPGAs.

VI. CONCLUSION

In this paper we showed how to measure temperature with digital methods and clarified that crosstalk induced delay in FPGAs is measurable. For this we used a simple circuit containing a ring oscillator and two counters. Relative temperature variations can be measured very precisely with errors less than 0.3 °C. For this result we investigated the standard deviations of measurements with different measurement times and a different number of delay elements in the ring oscillator.

To measure the delay changes caused by crosstalk effects nearly the same circuit was used. The main changes are the addition of aggressor nets and the manual routing of these. The presented measurement circuit is a very easy solution for post-production validation of programmable devices against crosstalk effects.

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