System level modeling of Networks-on-Chip for power estimation and design space exploration

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**Motivation – Trends**

**CMOS:**
- Higher transistor densities (Moore’s Law)
- Lower voltages and charges in memories
- High clock rates
- Increasing Design-Productivity-Gap
- (Heterogeneous) Multi Processor Systems-on-Chip (MPSoC)

**Reliability:**
- Ageing effects
- Timing and signal integrity
- Temperature dependence

**Power:**
- Constrained budget
- Imbalances
- Early estimation needed

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Main Topics

**Design on System Level:**
- Lift abstraction up to system level where possible
- Enable early design space exploration

**Power Estimation of Networks-on-Chip (NoC):**
- Characterize NoC for power annotation
- Generate power budgets and distributions at system level

**Thermal Simulation:**
- Thermal model in system simulation
- Temperature aware managing and task mapping
**System Level Simulation**

- **SystemC System Model and Simulation**
  - TLM, transaction objects
  - No clock signal but wait statements
  - Dynamic sensitivities
  - Cycle accurate
  - Speed Up
    - by 10 x – 90 x compared to RTL

![Graph showing simulation time and speed up](image)
Networks-on-Chip

- Many Core and System-on-Chip
  - Rising impact of communication architecture
  - Preferred solution: Networks-on-Chip
Networks-on-Chip

Here:

- Synchronous design
- XY-Routing
- Wormhole switching
- Mux crossbar
- Clock gating capabilities
Networks-on-Chip

Parameter set:

- NoC size -> 2x2 .. 10x10
- Different IP cores -> CPU, GPU, RAM, I/O, ...
- Link width -> 32 .. 128 bit
- #Buffers -> 1 .. 8 stages FIFO
- Frequency -> 100 .. 1000 MHz
- Technology node -> 65 .. 32 nm
- Different traffic situations -> task graph modeling, varying degrees of parallelism
Power Estimation of NoCs

Methodology:

- Technology Libraries
  - RTL/Behavioral
    - Synthesis
  - Short Test Bench
    - Gate-Level Simulation
    - Power Analysis

- Power Model

- Architecture, System Description, Task Graphs
  - System-Level Simulation

Simulation CHARACTERIZATION

Power Temperature Distribution Performance Data
Power Estimation of NoCs

Router Power Model:

- For all different parameters:
  - Static power consumption
  - Dynamic power consumption
    - Transferring no flit (idle)
    - Transferring 1 flit
    - Transferring 2 flits (for verification)

- Additional:
  - Area
  - Max. frequency
Power Estimation of NoCs

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**Results:**
- Technology characterization

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**Diagram:**
- Power in µW vs Frequency in MHz
- Linear as expected
- # active Ports
- 0
- 1
- 2

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**Router**
- @
- 65 nm
- 32 bit
- 1 Buffer

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Power Estimation of NoCs

Results: technology - NoC Architecture characterization

100 MHz
32 bit
1 Port active

Router

Linear for FIFO > 1#

FIFO with 1#
Power Estimation of NoCs

System
@ 100 MHz
64 bit
65 nm

Sweet Spots

Energy-Delay-Product [e-12Js]

Number of Cores

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Thermal Simulation

- Power dissipation results in heat generation
- Thermal modeling of MPSoCs
- Proactive estimation of thermal distribution during design and runtime
  - Enabling **Proactive Thermal Management** and **Thermal Aware Task Mapping**
Thermal Simulation

Tile Mapping

Current source

Chip

Spreader

Sink

Heat flow to ambience

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Thermal Mapping

Physical parameters → Temperature Modeling

- Prediction
- Temp. Map

→ Temperature profile

Predicted temperatures → Proactive Mapping, Reactive Mapping

→ Applications, Task Graphs

→ Next Mapping, Task properties

→ Mapping decisions

→ Temperature, Activities

Measurement → System Control

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Thermal Mapping

- Task Mapping algorithms:
  - NN: nearest neighbor
  - WL: work load distribution
  - P: proactive thermal aware
  - R: reactive thermal aware

- Applications:
  - Task graph 1: short tasks with small packets
  - Task graph 2: long tasks with big packets
  - Task graph 3: average parameters
Thermal Mapping

<table>
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<th></th>
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</table>
Thermal Mapping

![Bar chart showing system runtime in milliseconds for different task graphs.](chart.png)
Further Work

Thermal Mapping:
- Evaluate more sophisticated mapping strategies
- Fine tune parameters for clear results

Power Estimation:
- Improve power model of functional IP Cores
- Verification, Quantify accuracy

Conclusion:
- Fast design space exploration with power and temperature
- Temperature aware system management -> better reliability
Thanks for your attention!
Any Questions?

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