Dynamic Circuit Techniques in Deep Submicron Technologies: Domino Logic reconsidered

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Current Situation and Outlook

Issues of current and future technologies:
- Power dissipation, Power density, Leakage currents, Interconnects, Parameter variability, Costs, Crosstalk, Clock distribution, Productivity, Memory-Wall, Verification, Reliability, ...

<table>
<thead>
<tr>
<th>Chip Area</th>
<th>Power consumption</th>
<th>Performance</th>
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<tbody>
<tr>
<td>GPP (2X)</td>
<td>2-3X</td>
<td>~1.4X</td>
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"Power outperforms Performance."

Static CMOS
- Reliable
- Scalable
- Automated design tools available
- Good compromise of speed, size, power consumption

Static CMOS has been and still is the dominating circuit technique

Dynamic logic
- Fast
- Power hungry
- Susceptible to noise
- Difficult to implement

Continuously used to boost performance
E.g. Intel Pentium 4 (Deleganes, 2004)
IBM Power4 (Warnock, 2002)
Sun Sparc VII (Heald, 2000)

Implementation of Dynamic Logic Styles

- Single-rail Domino
- High-Speed Domino

- 90nm Technology (Infineon)
- Low Vth Transistor types

Results for Power, Delay, Reliability and Design-Flow

Comparison of Power and Delay:

Reliability is endangered and has to be costly monitored due to:
- Charge leakage
- Charge sharing
- Power supply noise
- Crosstalk
- Clock skew
- and more...

Possible Design-Flow:
- System Description
- Synthesis
- Logic Compressor
- Pipeline Organization
- Placement and Routing
- Library Transformation
- Clock Tree Inverter
- Fabrication

In cooperation with:
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