Dynamic Circuit Techniques in Deep Submicron Technologies: Domino Logic reconsidered

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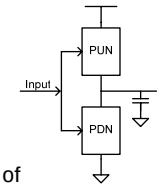
Current Situation and Outlook

Static CMOS

- Reliable
- Scalable
- Automated design tools available
- Good compromise of speed, size, power consumption



Static CMOS has been and still is the dominating circuit technique

Issues of current and future technologies:

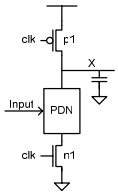
Power dissipation, Power density, Leakage currents, Interconnects, Parameter variability, Costs, Crosstalk, Clock distribution, Productivity, Memory-Wall, Verification, Reliability, ...

	Chip-Area	Power consumption	Performance
General Purpose Processors (GPP)	2X	2-3X	~1.4X

„Power outperforms Performance."

Dynamic logic

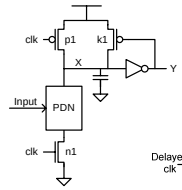
- Fast
- Power hungry
- Susceptible to noise
- Difficult to implement



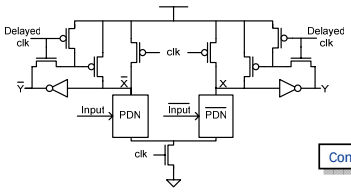
Continuously used to boost performance

E.g. Intel Pentium 4 [Deleganes, 2004]
IBM Power4 [Warnock, 2002]
Sun Sparc V9 [Heald, 2000]

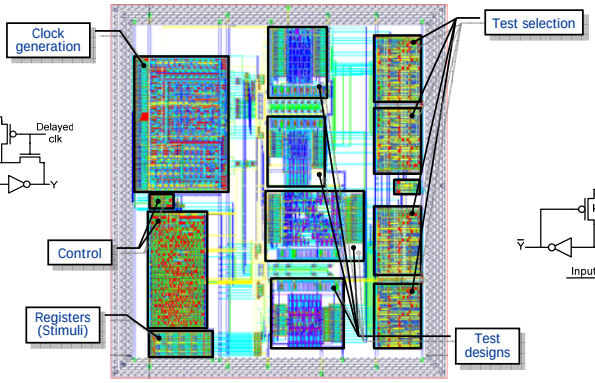
Implementation of Dynamic Logic Styles

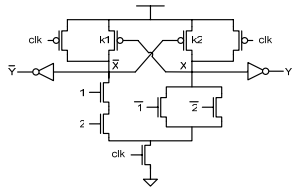


Single-rail Domino

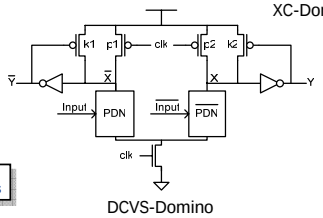


High-Speed Domino





XC-Domino



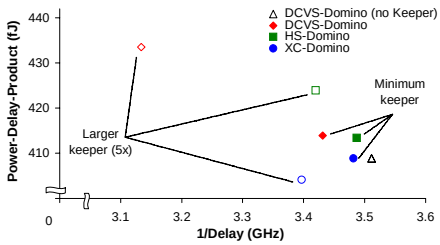
DCVS-Domino

- 90nm Technology (Infineon)
- Low V_{th} Transistor types

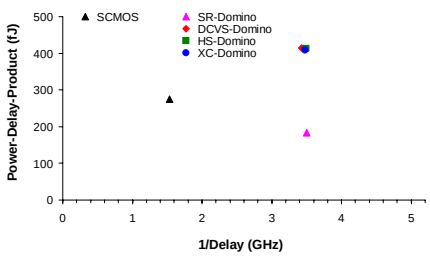
Results for Power, Delay, Reliability and Design-Flow

Comparison of **Power and Delay:**

a)



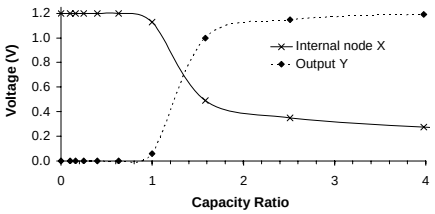
b)



Reliability is endangered and has to be costly monitored due to:

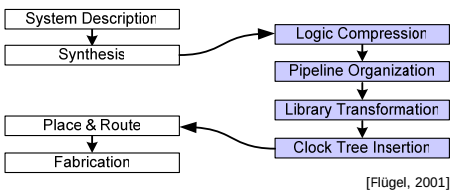
- Charge leakage
- Charge sharing
- Power supply noise
- Crosstalk
- Clock skew

and more ...



$$\text{Capacity Ratio} = \frac{\text{PDN's internal capacitance}}{\text{Capacitance of the dynamic node}}$$

Possible **Design-Flow:**



[Flügel, 2001]

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