Dynamic Circuit Techniques in Deep Submicron Technologies: Domino Logic reconsidered

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ABSTRACT
Dynamic circuit techniques offer potential advantages over static CMOS. Domino circuits are the most widespread representative in high performance designs but suffer increasingly from deep submicron effects. This paper presents evaluations in terms of area, power dissipation, and propagation delay for static CMOS as well as for several Domino derivatives in a 90 nm technology. Finally, issues of reliability gained from practical experience for different testbenches are discussed.

1. INTRODUCTION
For the last decades static Complementary Metal Oxide Semiconductor (CMOS) logic has been the dominating technique for the design of integrated circuits. Reliable, scalable, and robust functionality paired with automated design flows has been the key for success. Static CMOS offers good performance but cannot keep up with dynamic logic styles in terms of propagation delay [1]. Though, the shorter delays mostly have to be traded off for increased power dissipation or reduced noise margins [2][3]. Nevertheless, dynamic logic has effectively been used to boost critical paths in subsystems such as arithmetic units, large multiplexers, or register files. A dynamic logic that is widely utilized for this purpose is the Domino logic [4] and its many derivatives. Domino logic is for instance employed in the IBM PowerPC, the Intel Pentium 4, and the Sun UltraSPARC.
Current deep submicron technologies with gate lengths smaller 100 nm confront us with serious changes and new challenges in system design. Leakage currents increase drastically and will make static power consumption the dominating fraction of the total power dissipation. An analogue trend can be seen for interconnects influencing more and more the overall system performance [5]. Another issue to be mentioned here is the boost of costs for development and production. Against the background of these changes it needs to be reconsidered if Domino logic can be a solution for the above mentioned issues or if reliability problems due to leakage prohibit its future use. Section 2 introduces some Domino logic styles that are examined in this paper. The simulation setup is described in section 3 before the results are depicted and conclusions are drawn in section 4 and section 5, respectively.

2. DYNAMIC CIRCUIT TECHNIQUES
Dynamic circuit techniques are the fastest commonly used circuit family. They avoid the large input capacitance of static CMOS, as a result of the pFETs, by using a clocked pull-up transistor. Figure 1 a) depicts a simple dynamic gate. The mode of operation can be divided into precharge and evaluation phase. The signal clk is low during precharge and the dynamic node X is charged high through transistor p1. When clk goes high the evaluation starts and X can be discharged through the Pull Down Network (PDN) and transistor n1. If the PDN does not provide a path to ground, X will be floating, storing the high signal on the parasitic capacitance. This floating state makes the node X sensitive to noise and is the cause for a possible malfunction. When dynamic gates as in figure 1 a) are cascaded very exact timing is needed both for the gate delays and the clock scheme to avoid failure as well as increased power consumption. However, such a successful setup can be achieved in a full custom design and results in very short propagation delays [6]. This option is not considered any further because the timing requirements can not be brought in line with increasing design complexity, parameter variations, and the need for automated design flows in future technologies.
In the following a gate with transistor n1 is called footed and is called unfooted when n1 is omitted.

2.1 Domino
An inverter is added to the output and assures the correct operation in a chain of cascaded gates as shown in figure 1 b). Furthermore the inverter drives the wire load as well as the input capacitance of the subsequent gate(s) and encapsulates the dynamic node X. This circuit technique is called single-rail Domino and only non-inverting functions can be implemented. Another modification is the additional pFET k1 connected to the

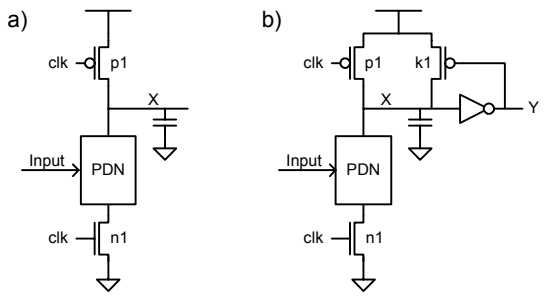

Figure 1 a) Dynamic and b) Single-Rail Domino gate

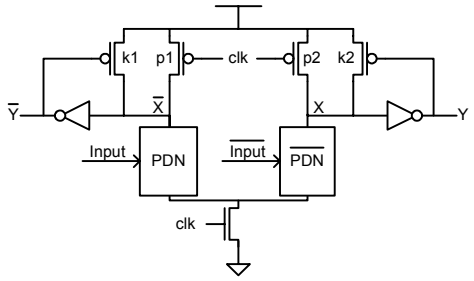

Figure 2 Footed DCVS-Domino

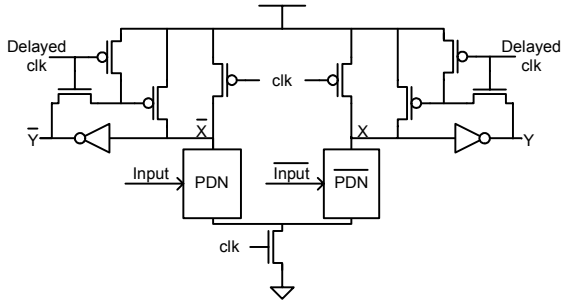

Figure 3 Footed HS-Domino using extended keeper

dynamic node X and the output Y resulting in an optional path to the supply voltage. This so called keeper can compensate charge loss when node X is floating. But the keeper is also the cause for short circuit currents and performance reduction because k1 is momentarily still turned on when the PDN starts to discharge the node X.

2.2 DCVS-Domino

The shortcoming of only non-inverting functions is overcome by the Domino derivate of the Differential Cascode Voltage Switch (DCVS) logic [7]. A gate is built of two complementary PDNs and provides differential output signals (see figure 2). Transistors of both PDNs can be used jointly to implement complex logic functions very efficiently. The general disadvantage of differential structures is that one node is discharged every cycle independent of the input signals.

2.3 HS-Domino

The introduced keeper causes short circuit currents as mentioned in section 2.1. Allam et al. [8] propose a technique to avoid this contention by turning the keeper on after the evaluation is ready. This is obtained by an extended keeper structure controlled by a delayed clock signal (see figure 3). Indeed the short circuit currents can be avoided but at the cost of increased area demand for the additional inverters as well as for the routing and the generation of the delayed clock signal. Besides, the extra clock signal also increases the power consumption.

2.4 XC-Domino

The last examined derivative is Cross-coupled (XC) Domino [2]. The difference to DCVS-Domino is that the gates of the keepers are connected to the opposite dynamic node and not to the outputs of the corresponding inverters. The short circuit currents are

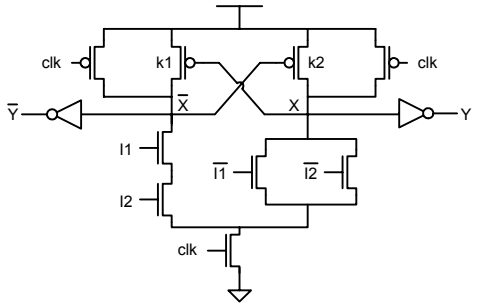

Figure 4 Footed Cross-coupled (XC) Domino

avoided because the keepers are turned on after the evaluation is ready, in contrast to HS-Domino without any additional effort. An implementation of a footed NAND2 with XC-Domino is shown in figure 4. It needs to be mentioned that in the case of faulty timing the dynamic nodes can possibly float when the evaluation has started and no valid input signals have arrived in the given time frame. In that case all input signals will be low and the dynamic nodes are neither connected to ground nor to the supply voltage. This scenario also defines a minimum clock frequency.

3. SIMULATION SETUP

Most circuit techniques can be accelerated in a wide range by simply applying larger gate widths to the transistors. But the applicability of the physical layout limits the gate widths to realistic values. For this reason we limited the maximum gate width to 25 times the minimum gate width for pFETs as well as nFETs and defined the maximum wire load to be equivalent to routing across 125 average cells of the corresponding circuit technique. To reproduce the worst-case scenario under the given constraints, we looked for a first testbench that should be easy to validate. As the delay of a single gate is not a good measure to compare circuit techniques we used a chain of six NAND4 and NOR4 gates connected alternately as inverters with the specified maximum wire load. In this case the output of each gate has to be discharged via the series of transistors representing the critical path (e. g. via I1 and I2 for the NAND2 in figure 4). The simple Domino logic cannot implement inverting functions (see section 2.1) so that we set up a comparable testbench of AND4 and OR4 gates for this circuit technique. To have another more realistic testbench with varying wire loads and fan-in, we designed a 4x4 bit Wallace tree multiplier. Both testbenches were surrounded by registers for the input and output signals to consider a setup in a pipeline structure or the interface to static logic, respectively.

All simulations were performed for the 90 nm technology from Infineon Technologies AG. The transistors were of type low threshold voltage (LVT) to achieve high performance and to better observe the influence of noise as the cause for failure. Additional parasitic capacitances, due to intra-cell interconnects, overlapping diffusions etc., were added to the

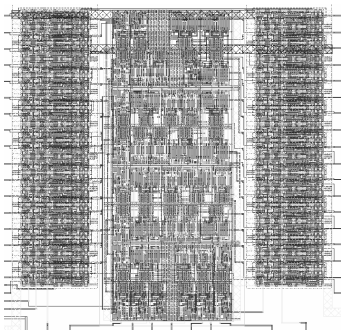

Figure 5 Layout of the Wallace tree multiplier

schematics to map the behavior of the layout as accurate as possible. All circuit techniques were dimensioned similarly to gain a fair comparison. The inverters influence the gate delay the most. Though, the PDNs also have significant effect on the gate delay so that the inverters as well as the PDNs were sized to the defined upper limit. The pFET clock transistors were sized with equal driver strength as the PDNs and the keepers were initially of minimum size. A shorter gate delay can be achieved by using unbalanced gates. For example the gate widths of the inverters' nFET can be made smaller. This reduces the evaluation delay and therefore the latency of the system due to a decreased capacitive load. But the precharge delay is increased resulting in smaller throughput and reduced noise margins so that this option is not considered further. The most promising circuit techniques were finally also implemented in the layout to perform post-layout simulations and to validate the results on a test chip. For instance the layout of the 4x4 bit Wallace tree multiplier in DCVS-Domino logic is depicted in figure 5.

4. RESULTS

This section presents and discusses the results for the introduced circuit techniques and testbenches. The pre- and post-layout simulations did not differ much due to the parasitic capacitances already included in the schematics. Thus, there is no need for a separate discussion. All data shown was obtained under the maximum achievable frequency and a fixed adjusted clock delay. The clock delay is the delay of the clock signal between a gate and its successor. The values for the area, given in table 1, were derived from the accumulated cell sizes for the chain of NAND-NOR gates. But this testbench does not account for the possibility of differential gates to effectively implement complex functions or the fractional assignment of single-rail gates. For example, the area for the Wallace tree multiplier was in our case nearly the same as for static CMOS but values of only 85 % area demand have also been reported [2].

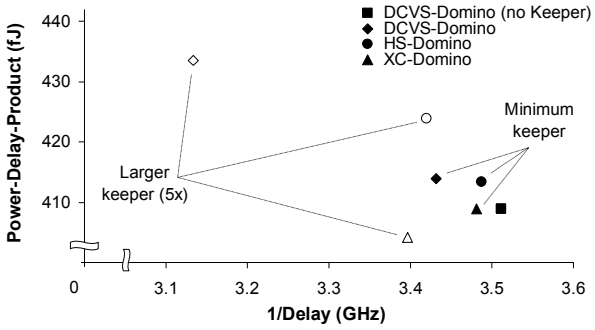

Figure 6 Performance comparison of Domino circuits

4.1 Performance and Power

Figure 6 depicts the results of the NAND-NOR chain for the various examined differential circuit techniques and table 1 resumes the results in comparison with static CMOS and single-rail Domino. The diagram represents the Power-Delay-Product (PDP) over the reciprocal of the delay to be able to set the power consumption in relation to the delay. So a result far right and down represents a high performance circuit technique consuming a disproportionably amount of power. The differential techniques do not deviate much when the keepers are kept at minimum size (filled out markers). The delay only varies 2.3 % while the PDP is within a 1.3 % interval. But when the keepers are enlarged to five times the minimum size (bordered markers) the techniques differ up to 12 % and 7.3 % for the delay and the PDP, respectively. DCVS-Domino without a keeper is the fastest logic because it does not add any additional capacitive load whereas DCVS-Domino with a keeper has to pay off for the short circuit currents in terms of delay and power consumption. HS-Domino and XC-Domino are nearly equally fast with a power advantage of XC-Domino as a result of the keeper's overhead in HS-Domino.

The measured power dissipation does not consider the adjusted clock tree so that an extra 5 to 20 % have to be added depending on the clock scheme, distribution, and accurateness. All differential Domino techniques feature a similar clock load except for HS-Domino due to the overhead of the keeper structure. There are two possible ways to reduce the clock load. The first one is to use unfooted gates instead of footed gates to avoid the capacitance added by the nFET clock transistor. Unfooted gates gain performance compared to footed gates of about 5 % for a fan-out of four (FO4) and up to 15 % for average systems. But this performance gain comes along with an increase in power consumption of roughly 12 %. The reason is short circuit currents at the beginning and at the end of the precharge phase (clock=low) when valid input signals are still or already available at the inputs. The second possibility is not to supply every gate with an adjusted clock delay but to use the same clock signal for a group of gates. This corresponds to a zero clock delay and Domino techniques will in principle still work. However short circuit currents as described before will occur especially for unfooted gates causing an increase in power

Table 1 Comparison of Domino circuit techniques and static CMOS in a worst-case scenario

Circuit technique	Area	Power dissipation	Delay	Power-Delay-Product	Area-Delay-Product
Static CMOS	1	1	1	1	1
Domino (Single-Rail)	0.913	1.525	0.437	0.667	0.399
DCVS-Domino (no Keeper)	1.811	3.415	0.436	1.490	0.790
DCVS-Domino	1.826	3.379	0.446	1.508	0.815
HS-Domino	1.911	3.429	0.439	1.506	0.839
XC-Domino	1.826	3.386	0.440	1.490	0.803

consumption of up to 40 %. For footed gates the rise of power consumption is still noticeable but significantly smaller because the path to ground is as far as possible blocked by the nFET clock transistor.

4.2 Reliability

There are many issues that endanger the reliability of Domino circuits: Charge leakage, charge sharing, power supply noise, crosstalk, and clock skew just to name a few. As mentioned before Domino circuits can be clocked with varying clock delays so that clock skew is not a major issue. The same applies for signal loss as a result of leakage currents that can successfully be compensated by the different keeper structures. Admittedly, small keepers are not capable of compensating fast signal loss due to temporary low resistive paths. This might occur for power supply noise or when crosstalk on interconnects lifts the gate voltage of the PDNs above the threshold voltage. Charge sharing is another reason for failure. We simulated a possible scenario for a gate with a minimum sized keeper in DCVS-Domino. This is illustrated in figure 7 where the voltages of the dynamic node X and the output Y are presented over the capacity ratio. The ratio is derived by the internal capacitance of the PDN divided by the parasitic capacitance of the corresponding dynamic node. A ratio of 1.0 or larger causes a logical failure because the keeper can not compensate the charge loss before it is turned off by the changed output signal Y. A NAND4 has a ratio of about 0.7 so that gates with larger fan-in or complex gates with joint PDNs are susceptible to failure due to charge sharing. Possible solutions are to precharge the internal nodes of the PDNs with extra pFET clock transistors or to control the inputs in a way that the conventional clock transistor will also precharge all internal nodes. A more

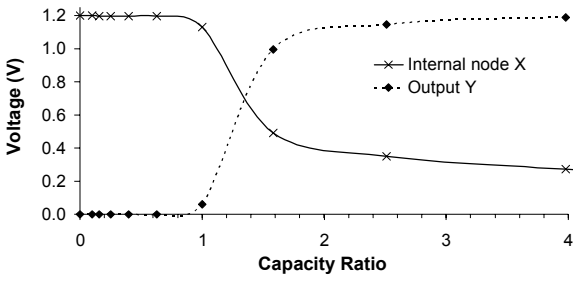

Figure 7 Critical capacity ratio for charge sharing

reliable system can also be attained up to a certain degree by increasing the keeper size but all solutions trade off reliability for power, area, and performance as shown in section 4.1. There are further issues like α-particles, substrate charge injection, and more that can not be covered briefly. Srivastava et al. [3] give a comprehensive overview of those issues and point out several methods to increase reliability.

5. CONCLUSION

Domino circuit techniques feature switching speeds out of range for static CMOS at the price of increased power dissipation and reduced noise margins. The reliability is endangered by deep submicron effects so that the electrical integrity has to be costly monitored and verified. For this reason and the lack of automated design tools Domino circuits will not be an alternative to CMOS for large integrated systems. Nevertheless they will still be an option to speed up critical units in the future deep submicron era when the constraints are considered.

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