Interconnects in on-chip Networks

Basics, solutions and future issues

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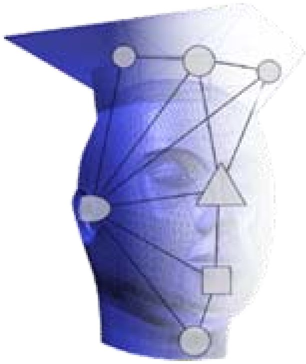
GRK-Workshop



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Department of Computer Science and Electrical Engineering

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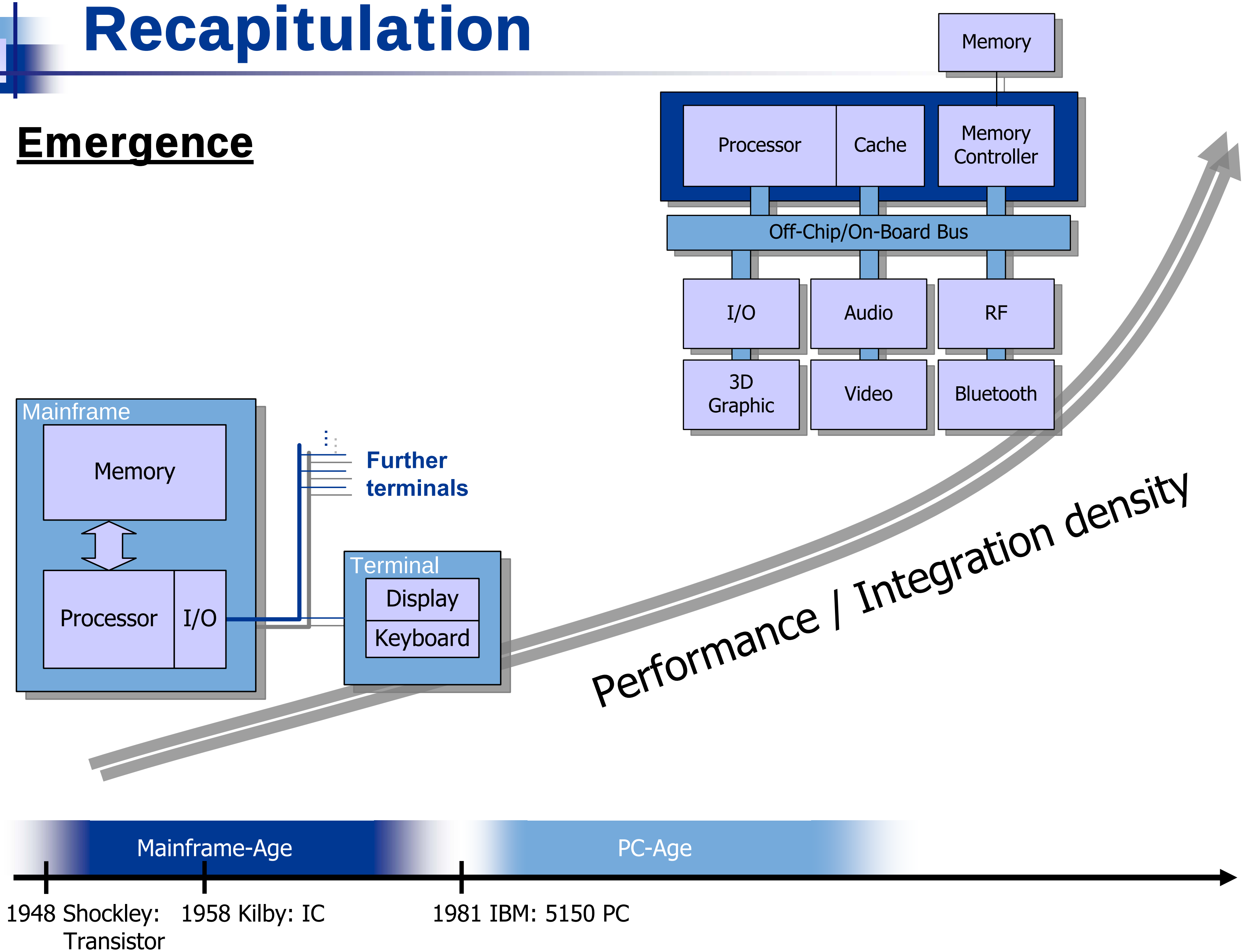
Outline

- Recapitulation
- Interconnect theory
- Design issues
- Further considerations
- Outlook

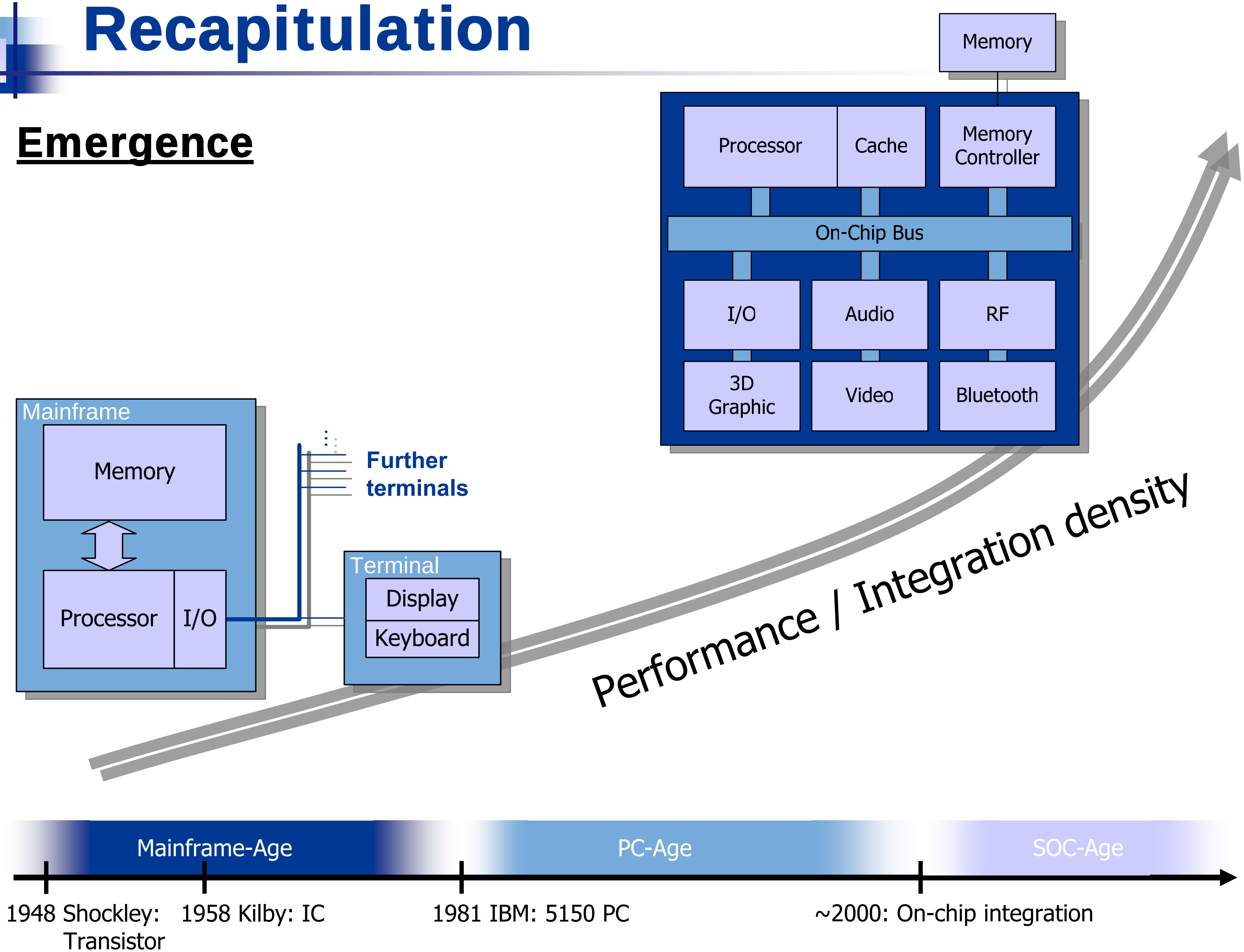
Recapitulation

Emergence



Recapitulation

Emergence

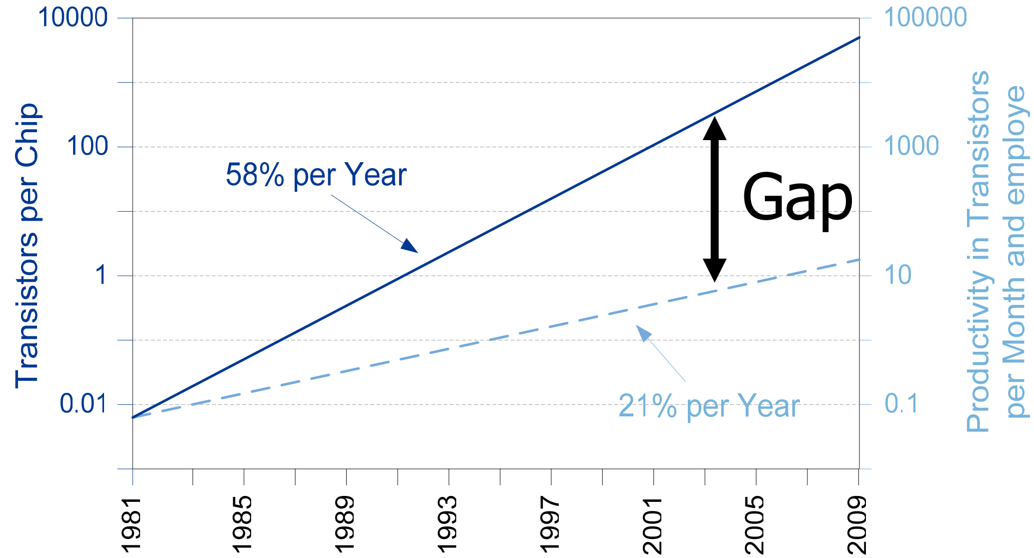


Recapitulation

Issues of current and future technology

- Power dissipation, leakage, power density
- Performance (frequency, MIPS)
- Design-Productivity-Gap
- Parameter variability
- Interconnects
- Reliability
- Costs

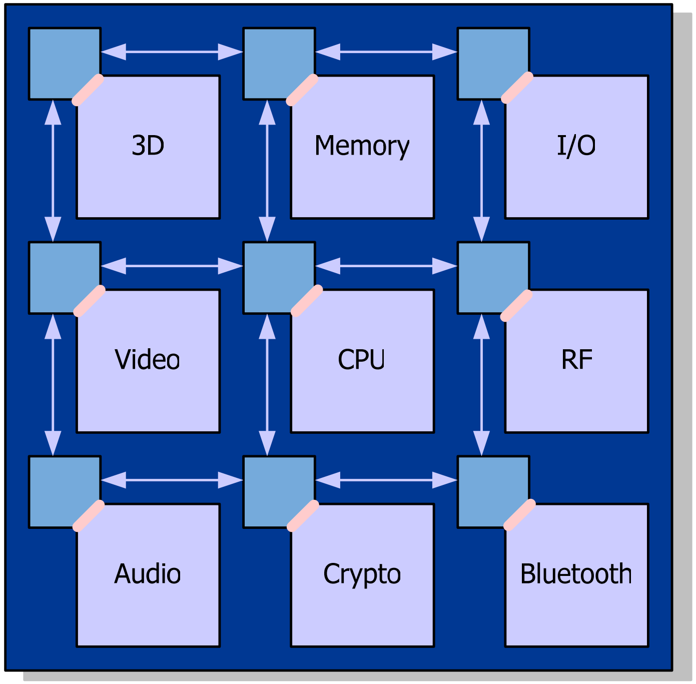
[ITRS, 1999]



We need more MIPS/mm² and more MIPS/Watt

Recapitulation

Network-On-Chip (NOC)



- Promising properties:
  - Modularity
  - Encapsulation
  - Portability
  - Reuse
  - Scalability
  - Parallelism
  - ...

- Optimists: More Moore (performance)
- Pessimists: More than Moore (issues of nanotechnology)

Change of Paradigms:

Computing-in-time → Computing-in-time-and-space

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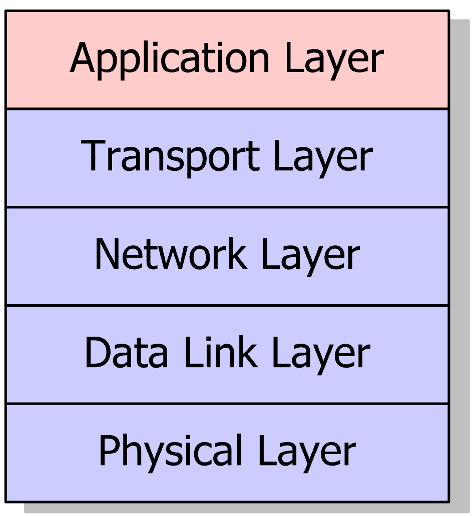
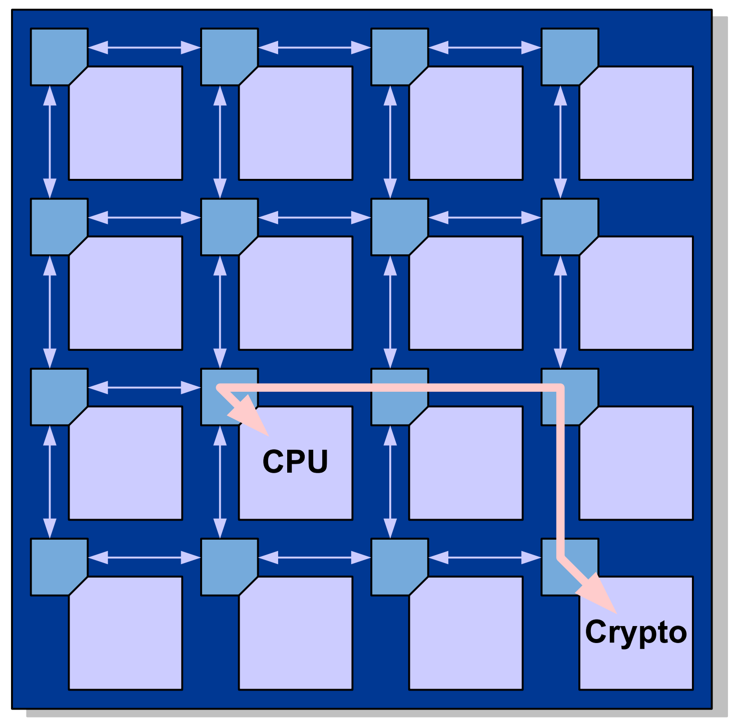
Recapitulation

Application layer

- Connection between applications
- Abstract application protocols:
  - Audio, Video, Crypto, Networking ...





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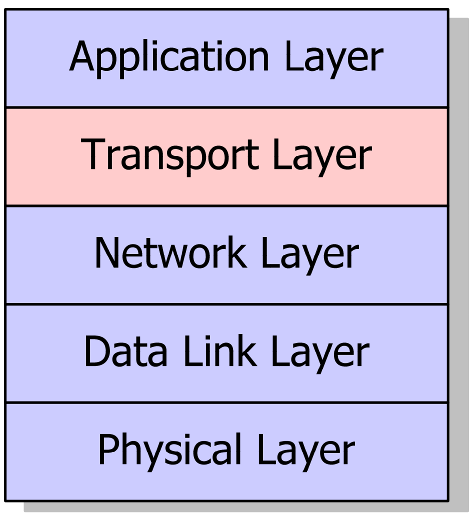
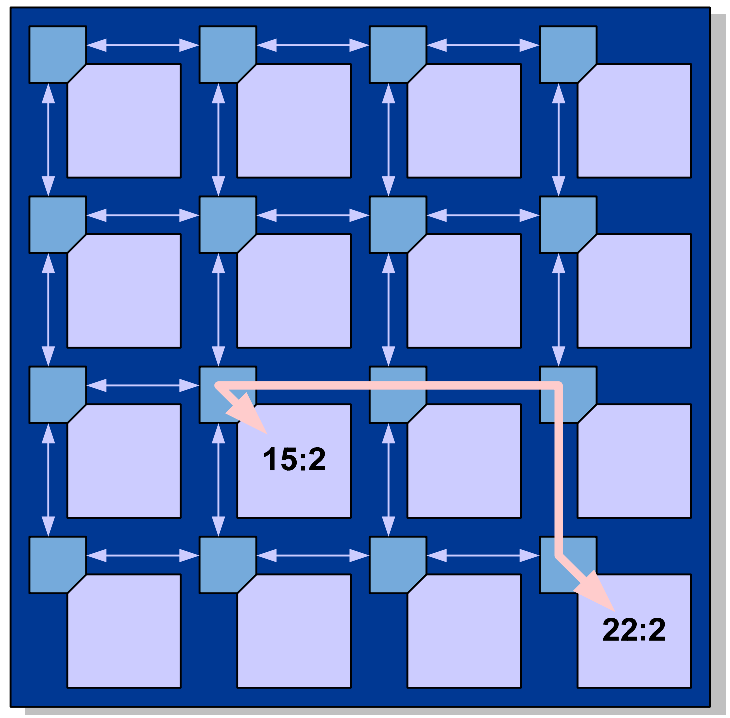
Recapitulation

Transport layer

- Point-to-point connection between resources/processes
- Connection-less and connection-oriented services
- Logical addressing and port numbers





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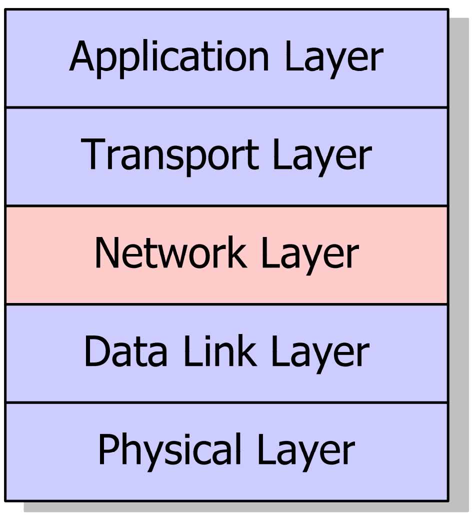
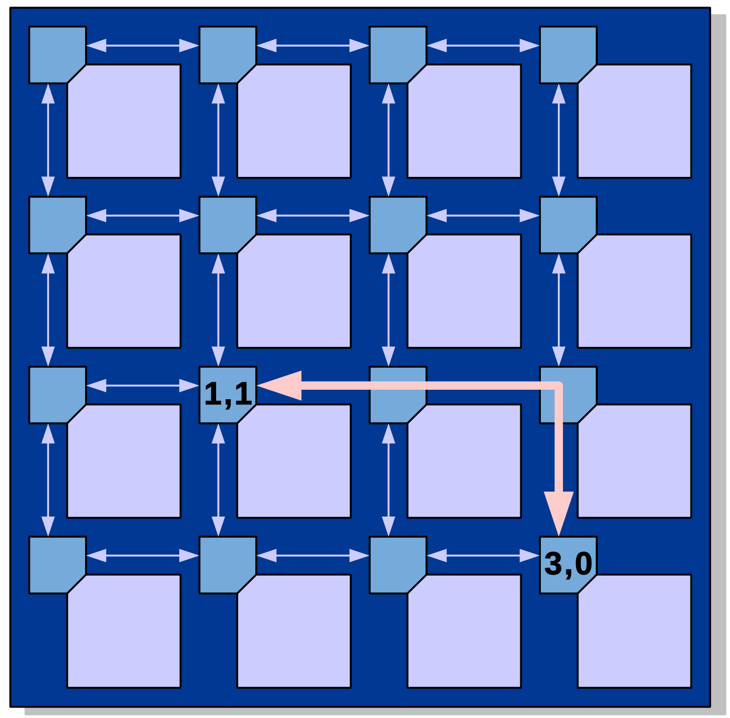
Recapitulation

Network layer

- Connection between distant routers
- Routing schemes:
  - Deterministic, Adaptive, Source-based, …
- Addressing:
  - Geographic, relative





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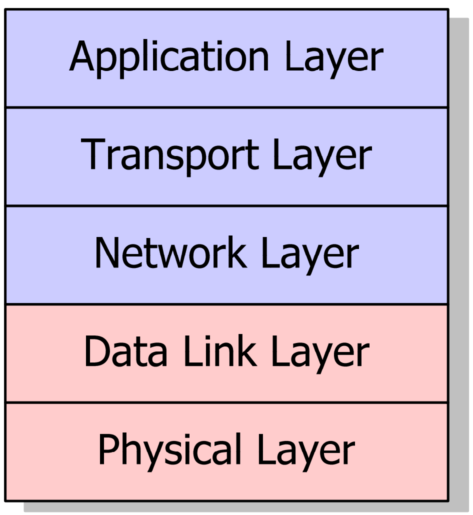
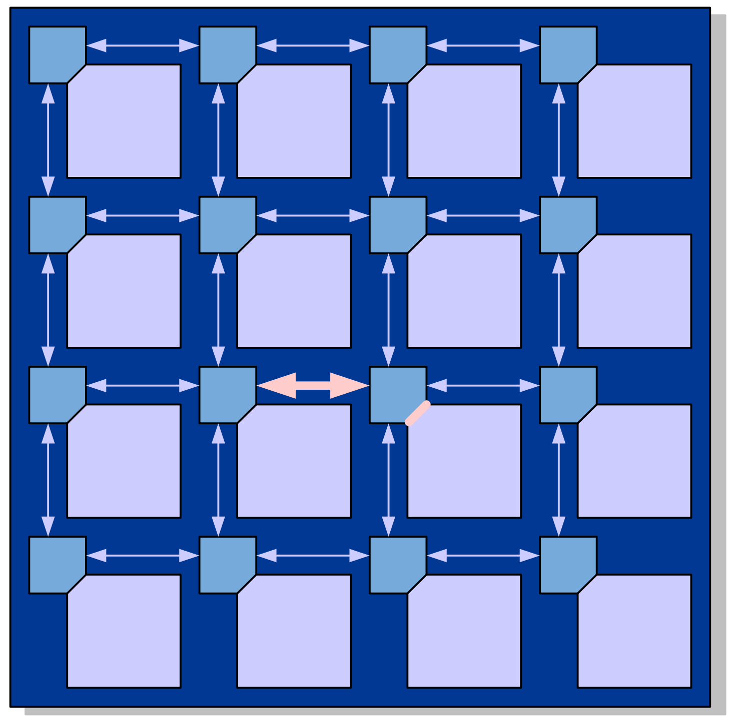
Recapitulation

Data Link and Physical Layer

- Connection between adjacent routers or router-resource
- Synchronization, Flow-control, Error-control
- Physical properties:
  - Voltage level, Data width
  - Modulation/Conversion





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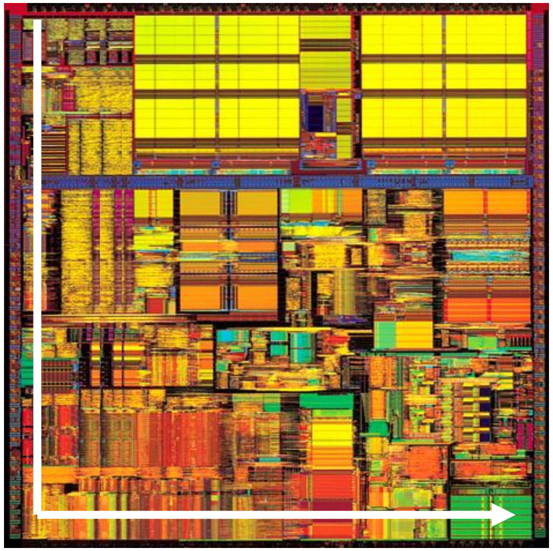
Interconnect theory

Propagation velocity

$$\mu_0 = 4\pi \cdot 10^{-7} \frac{\mathrm{V \cdot s}}{\mathrm{A \cdot m}} \qquad \varepsilon_0 \approx 8.854 \cdot 10^{-12} \frac{\mathrm{A \cdot s}}{\mathrm{V \cdot m}}$$

μ_0 Permeability of vacuum
ε_0 Permittivity of vacuum
μ_r Relative permeability
ε_r Relative permittivity

$$\boxed{v = \frac{1}{\sqrt{\mu_0 \mu_r \cdot \varepsilon_0 \varepsilon_r}} \approx \frac{0.3}{\sqrt{\mu_r \cdot \varepsilon_r}} \left[\frac{\mathrm{mm}}{\mathrm{ps}}\right]}$$



[Intel, 1999]

Example $\quad A_{\mathrm{chip}} = 576\ \mathrm{mm}^2 = (24\ \mathrm{mm})^2$

$$\mu_r = 1, \quad \varepsilon_r = 2 \quad \rightarrow \quad v \approx 0.2 \frac{\mathrm{mm}}{\mathrm{ps}}$$

$$d_{\mathrm{chip}} = 2 \cdot 24\ \mathrm{mm} \quad \rightarrow \quad t_{\mathrm{TOF}} = 240\ \mathrm{ps} \quad \hat{=} \quad f = 4.17\ \mathrm{GHz}$$

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Interconnect theory

Interconnects

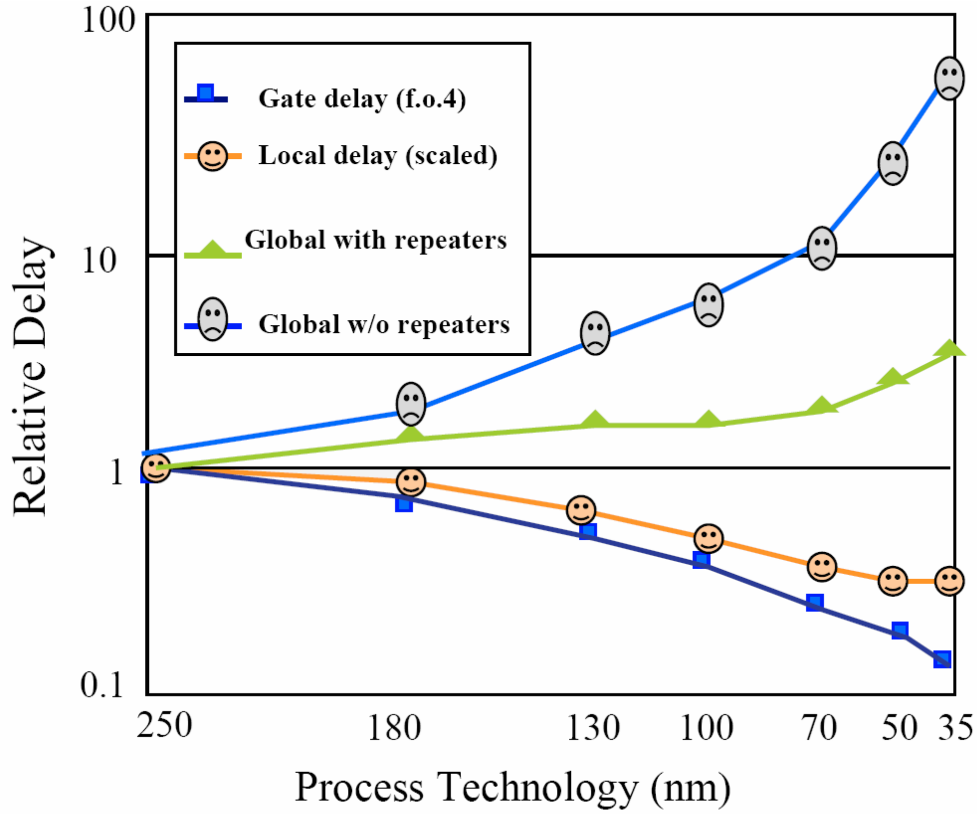
Propagation delays of global wires will be a multiple of the clock cycle.

Example (very optimistic):

6–10 clock cycles in 50 nm technology

[Benini, 2002]

[Tenhunen, 2005]



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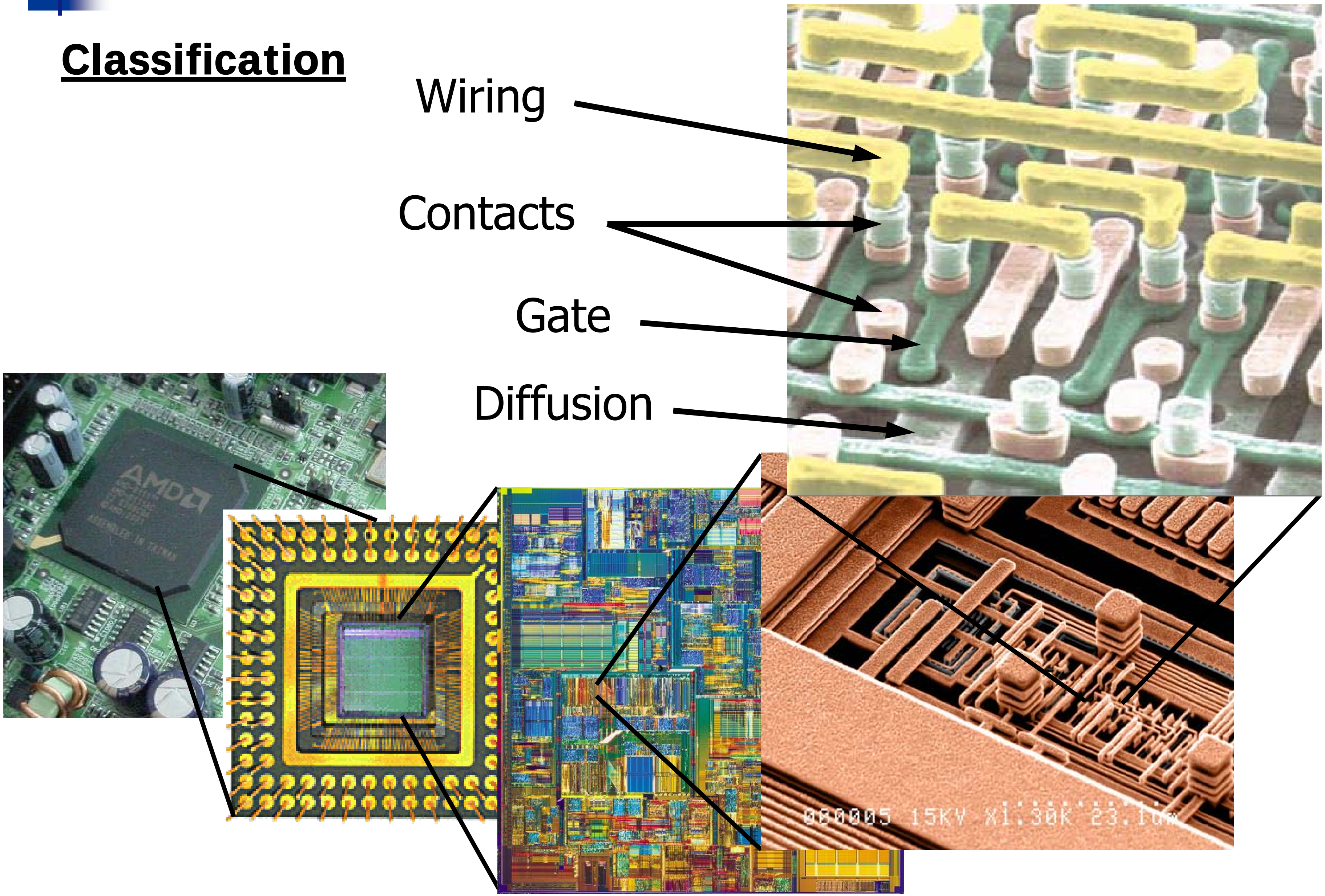
Interconnect theory

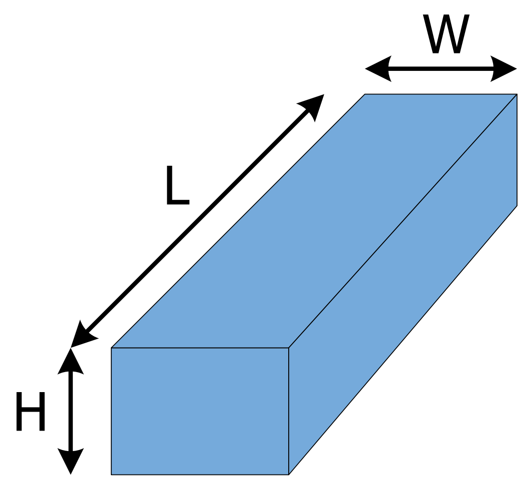
__Classification__



Interconnect theory

Resistance

$$R = \frac{\rho \cdot L}{H \cdot W} = R_{\square} \cdot \frac{L}{W}$$



Sheet resistance $$R_{\square} = \frac{\rho}{H} \quad \left[\frac{\Omega}{\square}\right]$$

$$\rho_{(\text{Aluminum})} = 2.8\ \mu\Omega \cdot \text{cm}$$

$$\rho_{(\text{Copper})} = 1.7\ \mu\Omega \cdot \text{cm}$$

Further aspects:

- Temperature dependency — $T \uparrow \;\Rightarrow\; R \uparrow$
- Frequency (Skin-effect) — $f \uparrow \;\Rightarrow\; R \uparrow$
- Contact resistance — 2-20 Ω (each)

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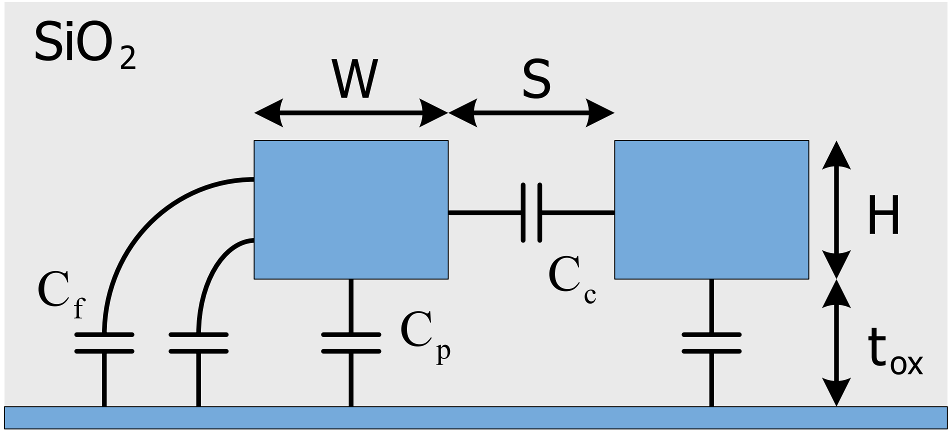
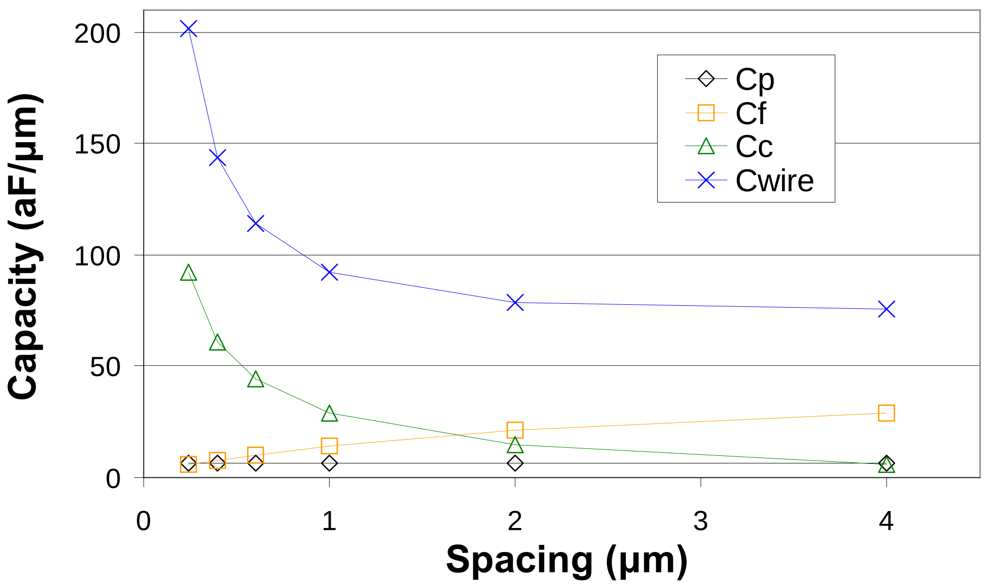
Interconnect theory

Capacitance

$$C = \varepsilon \cdot \frac{W \cdot L}{t_{ox}}$$

$$\varepsilon_{(\text{Silicon dioxide})} \approx 3.9 \cdot \varepsilon_0$$





C_p Parallel plate

C_f Fringing

C_c Crosstalk

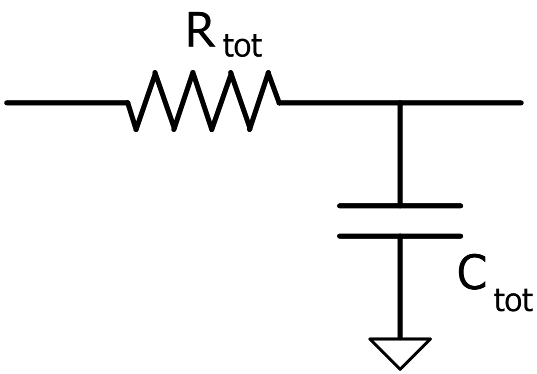
$$C_{wire} = C_p + C_f + C_c$$

Interconnect theory

RC-Delay

- Lumped model

$$\tau_{\text{wire 1}} = R_{\text{tot}} \cdot C_{\text{tot}}$$



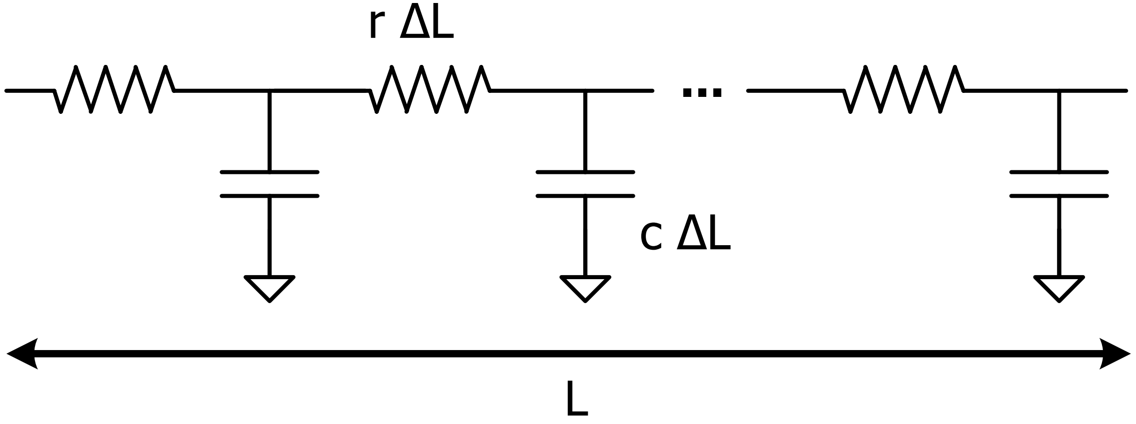
Inaccurate and pessimistic (especially for long wires)

- Distributed model

$$\tau_{\text{wire 2}} = r \cdot c \cdot L^2$$

$$R = r \cdot L$$

$$C = c \cdot L$$



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Design issues

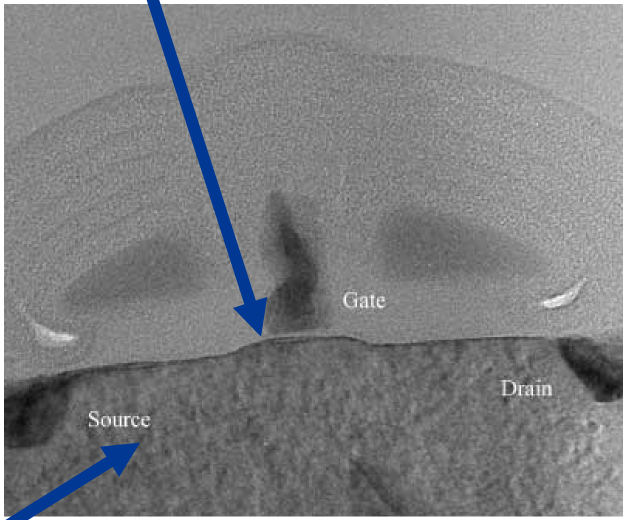
Technology scenario 2010

Technology node	45 nm
Chip size	620 mm²
Transistor count	4424 Mio.
Physical gate length	~20 nm
Metal layers	12-16
Frequency (global-local)	2-12 GHz
Total wire length	~2.2 km/cm²

- For M1-M6, 33% usage

[ITRS, 2003 and 2005]

<10 Ångström gate oxide thickness



[Intel, 2001]

<100 dopant atoms

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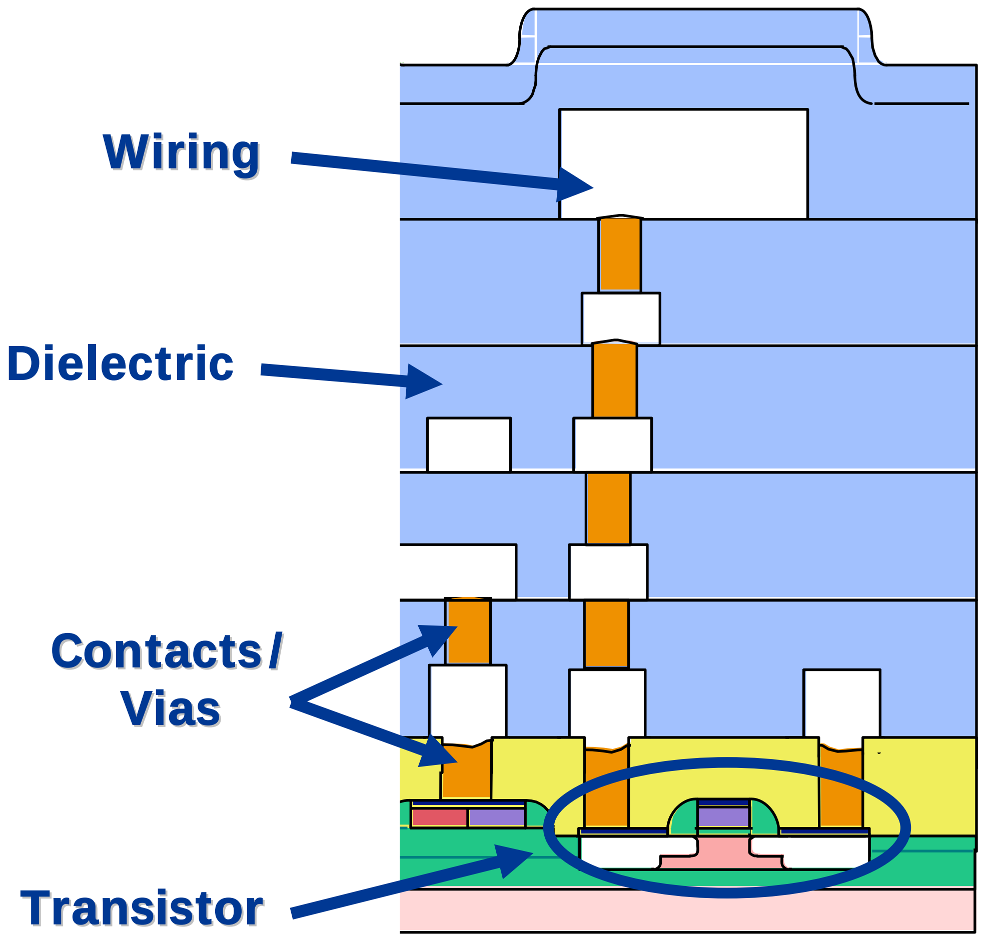
Design issues

Wire engineering

- Wiring material
  - Aluminum, copper …
- Dielectric
  - Oxide, Low-K, …
- Contacts and vias
  - Tungsten, copper, …
- Geometry
  - Height, width, spacing …

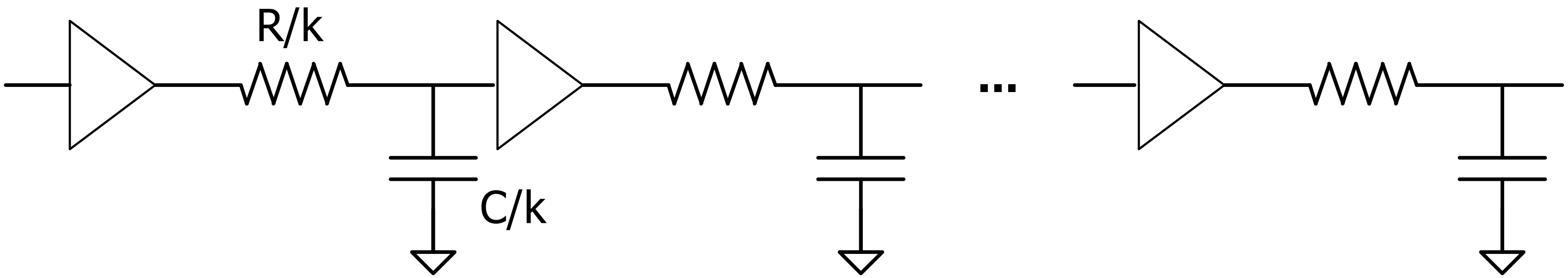


Design issues

Repeater

$$\tau_{\text{wire 3}} = k \cdot (\underbrace{t_{drv} + r \cdot c \cdot (L/k)^2}_{\text{constant}})$$

- Voltage mode
- Optimum placement is important
- Delay is linear with the length
- Large number of repeaters required



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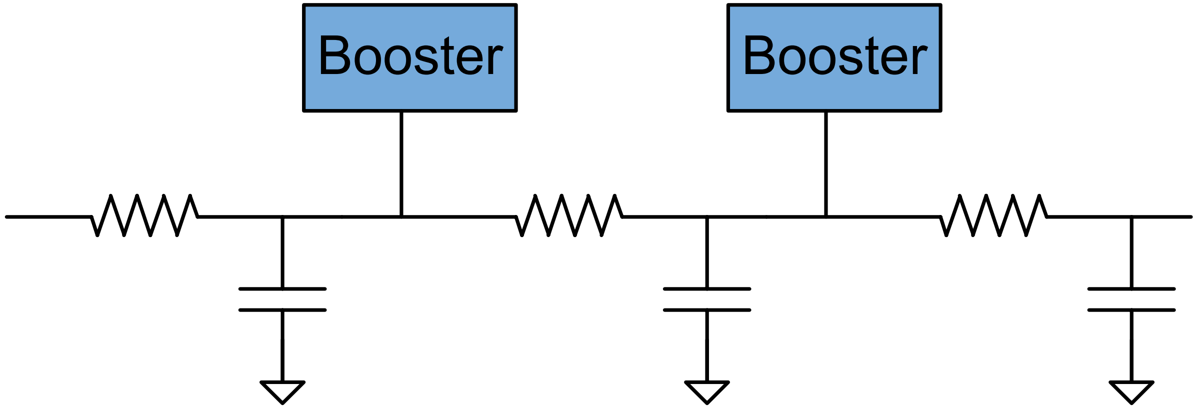
Design issues

Booster

- Sensing the wire for signal change
- Firing additional amplifier/booster
    - Voltage mode
    - Does not break the line
    - Cannot be pipelined
    - No tool-support (EDA)



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Design issues

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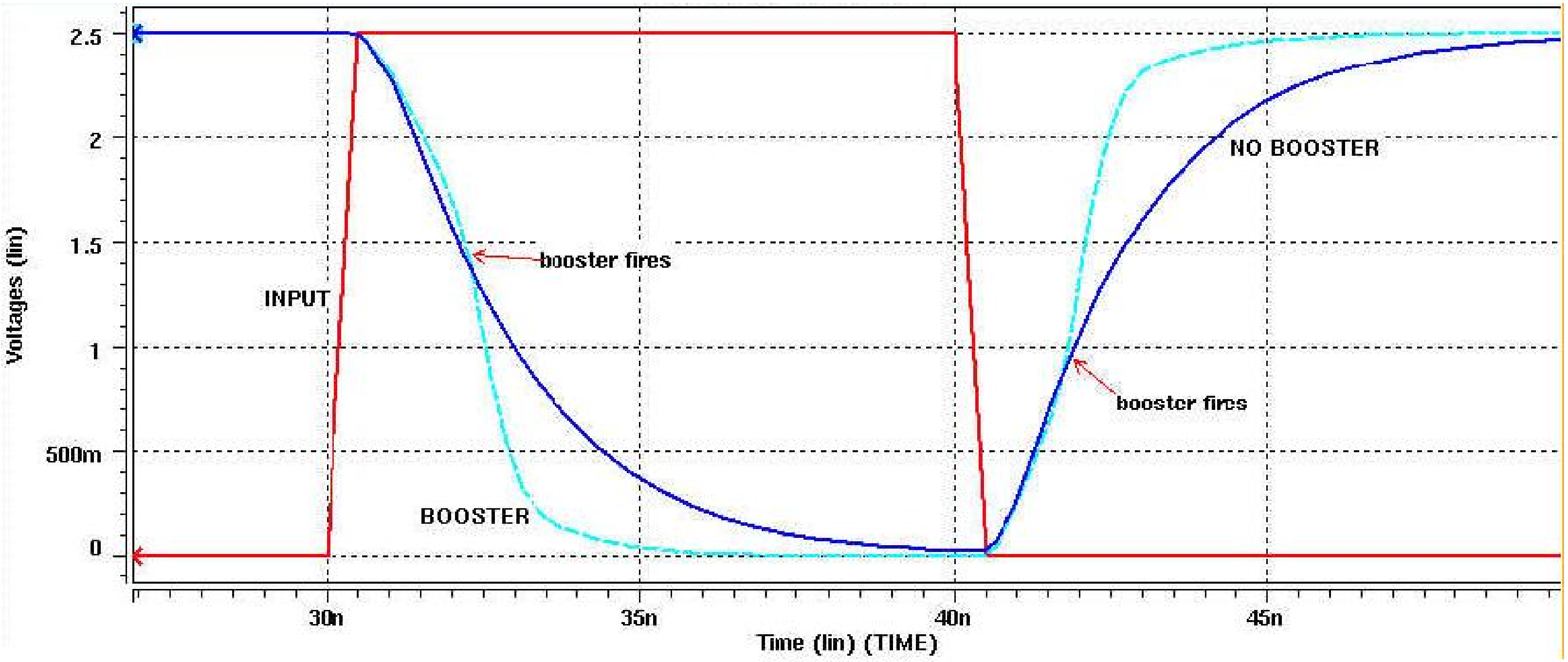

[Kukkamalla, 2003]

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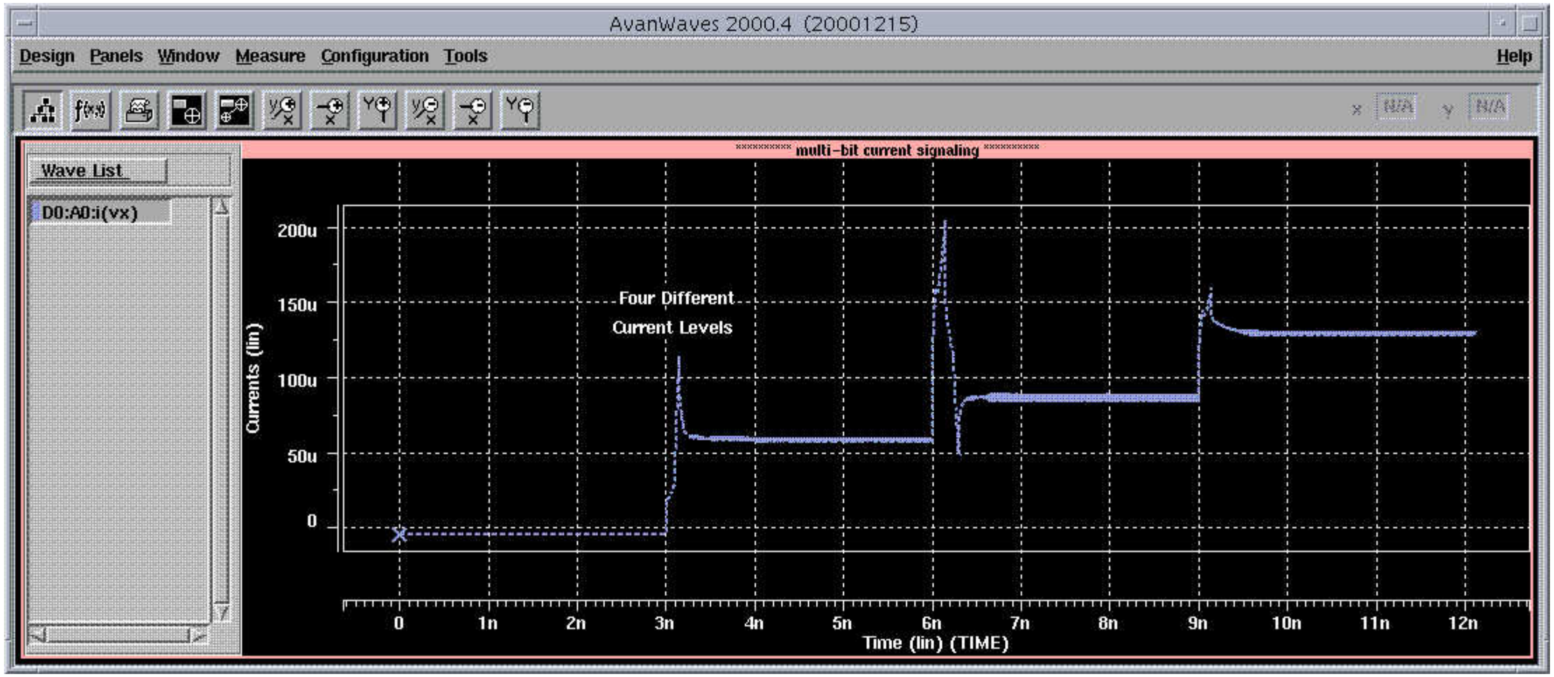
Design issues

Further design approaches

- Differential
- Low-swing
- Differential current sensing
- Multi-level current sensing

[Kukkamalla, 2003]



Design issues

<u>Further design approaches</u>

- Differential
- Low-swing
- Differential current sensing
- Multi-level current sensing
- Phase coding

  - Asynchronous
  - Wave pipelining
  - Hybrid-approach
  - Serial transmission
  - Optical interconnects
  - On-chip RF

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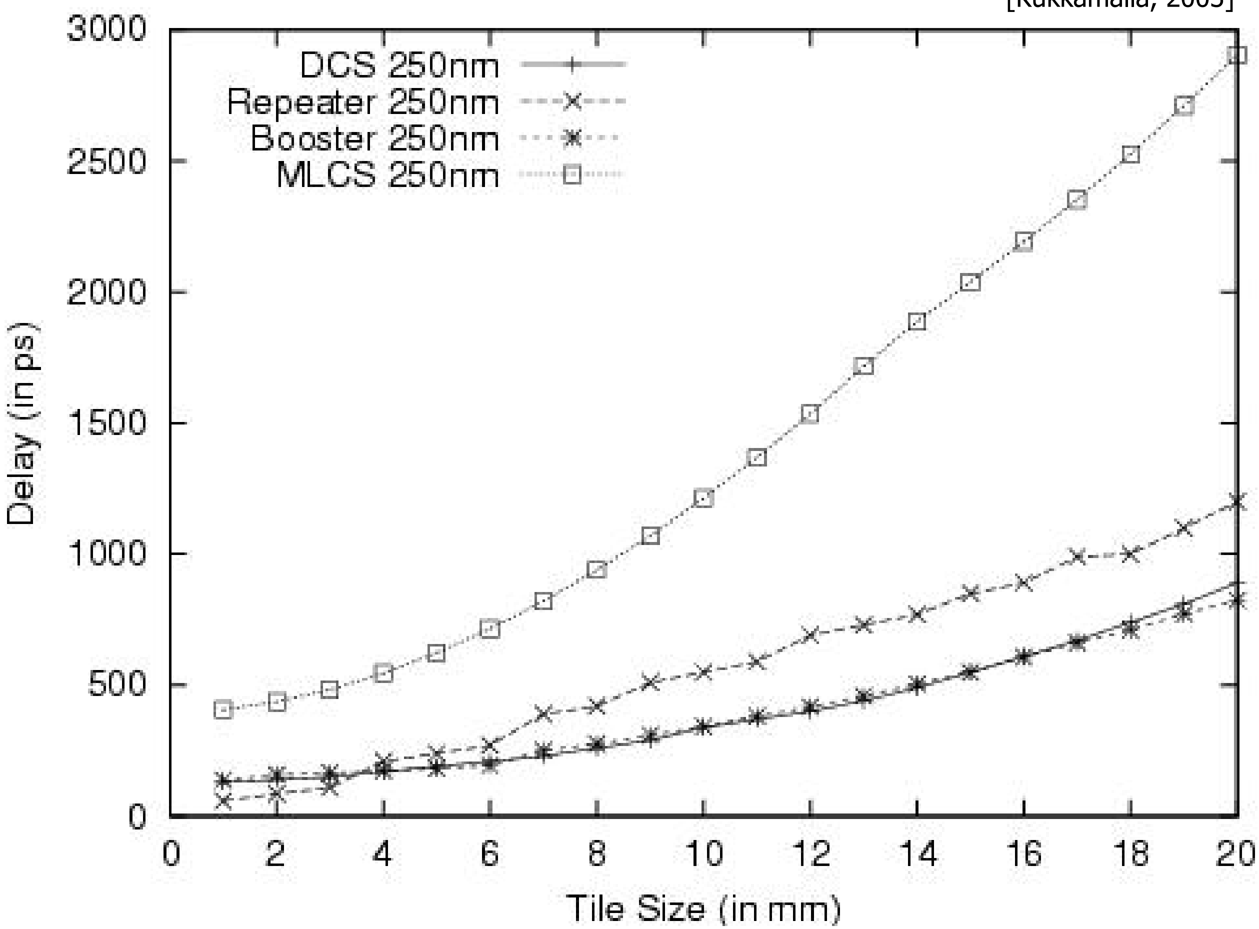
Design issues

Comparison

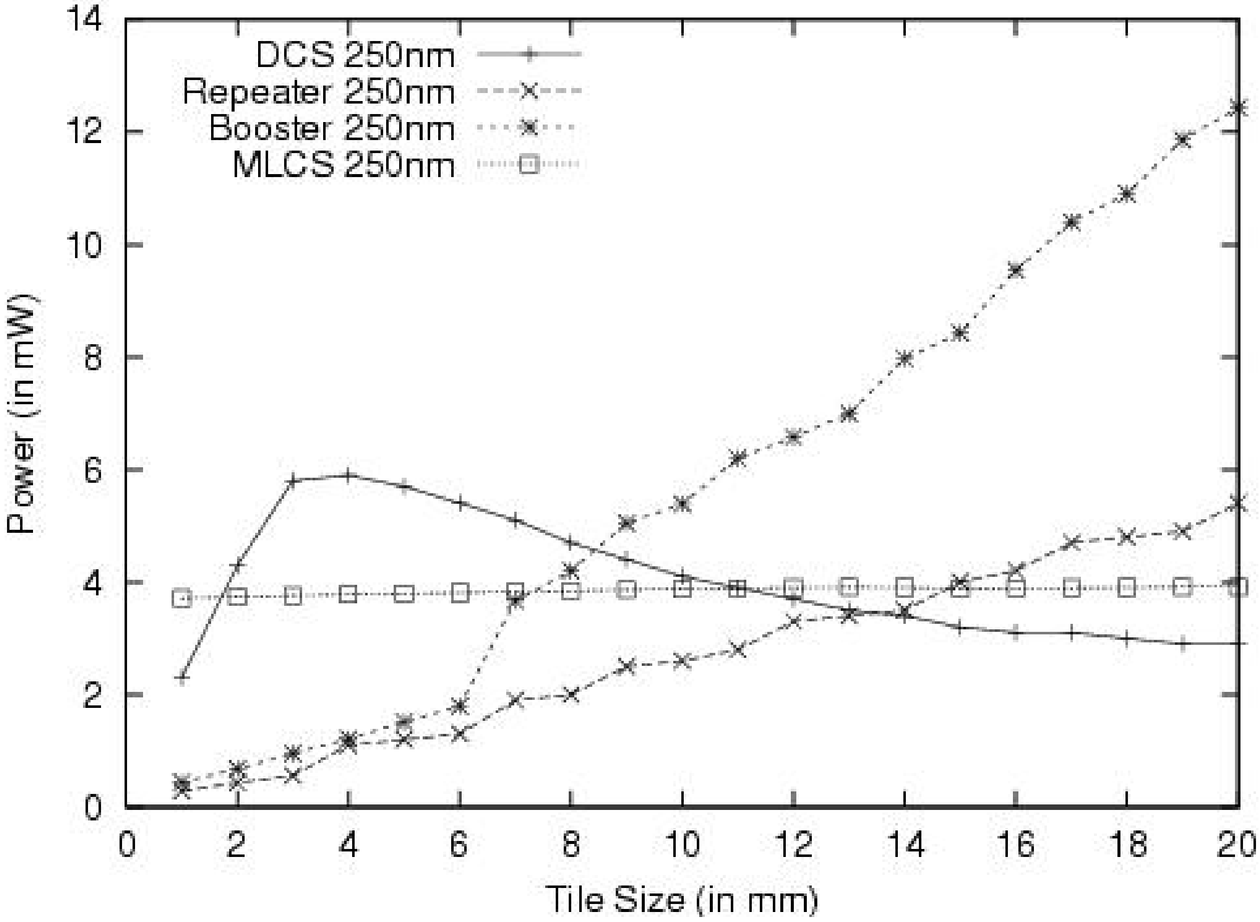
[Kukkamalla, 2003]



Design issues

Comparison

[Kukkamalla, 2003]



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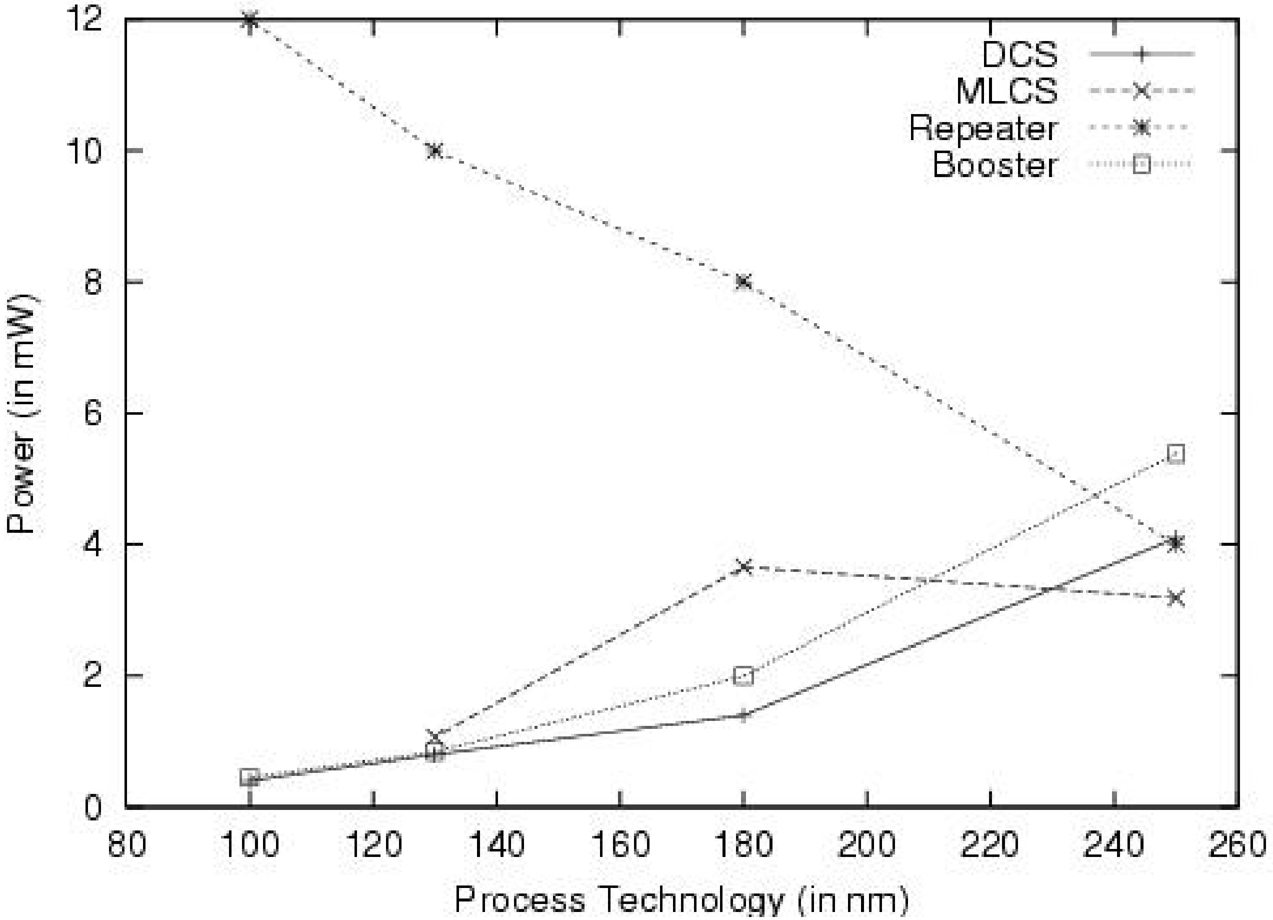
Design issues

Comparison

[Kukkamalla, 2003]



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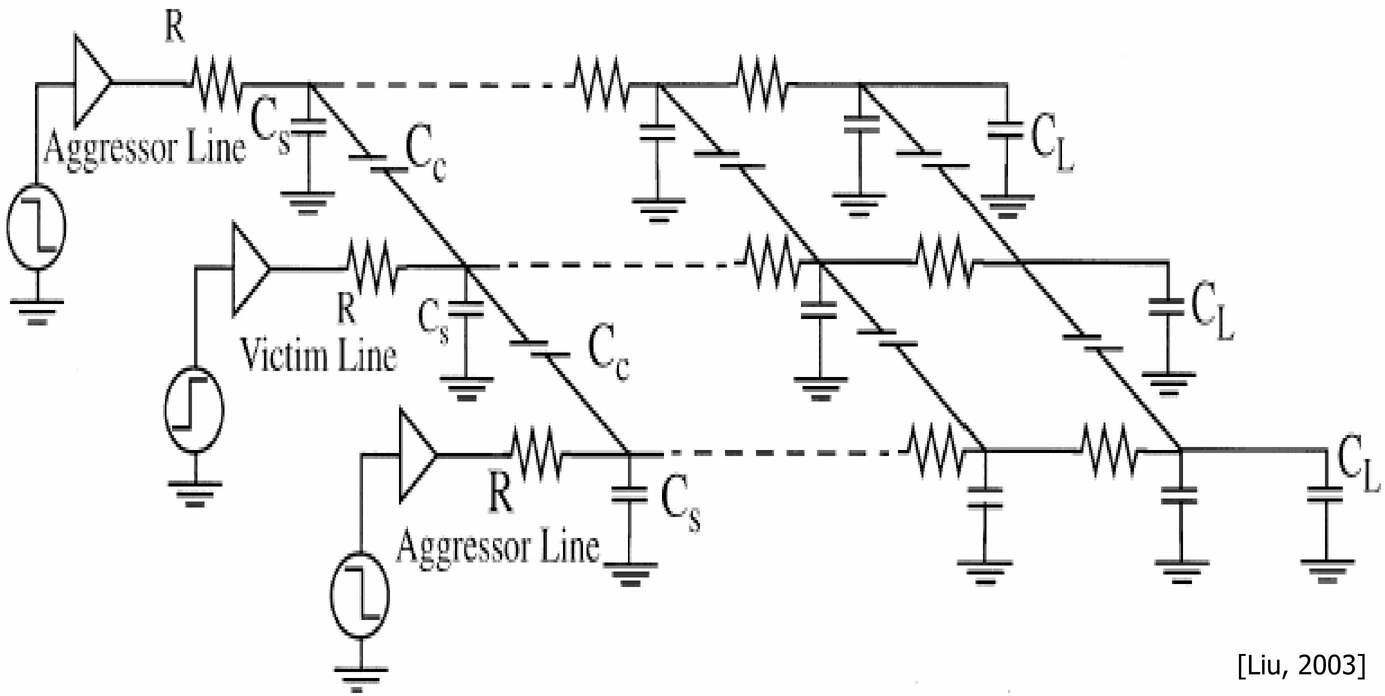
Further considerations

Bus / link model for crosstalk



[Liu, 2003]

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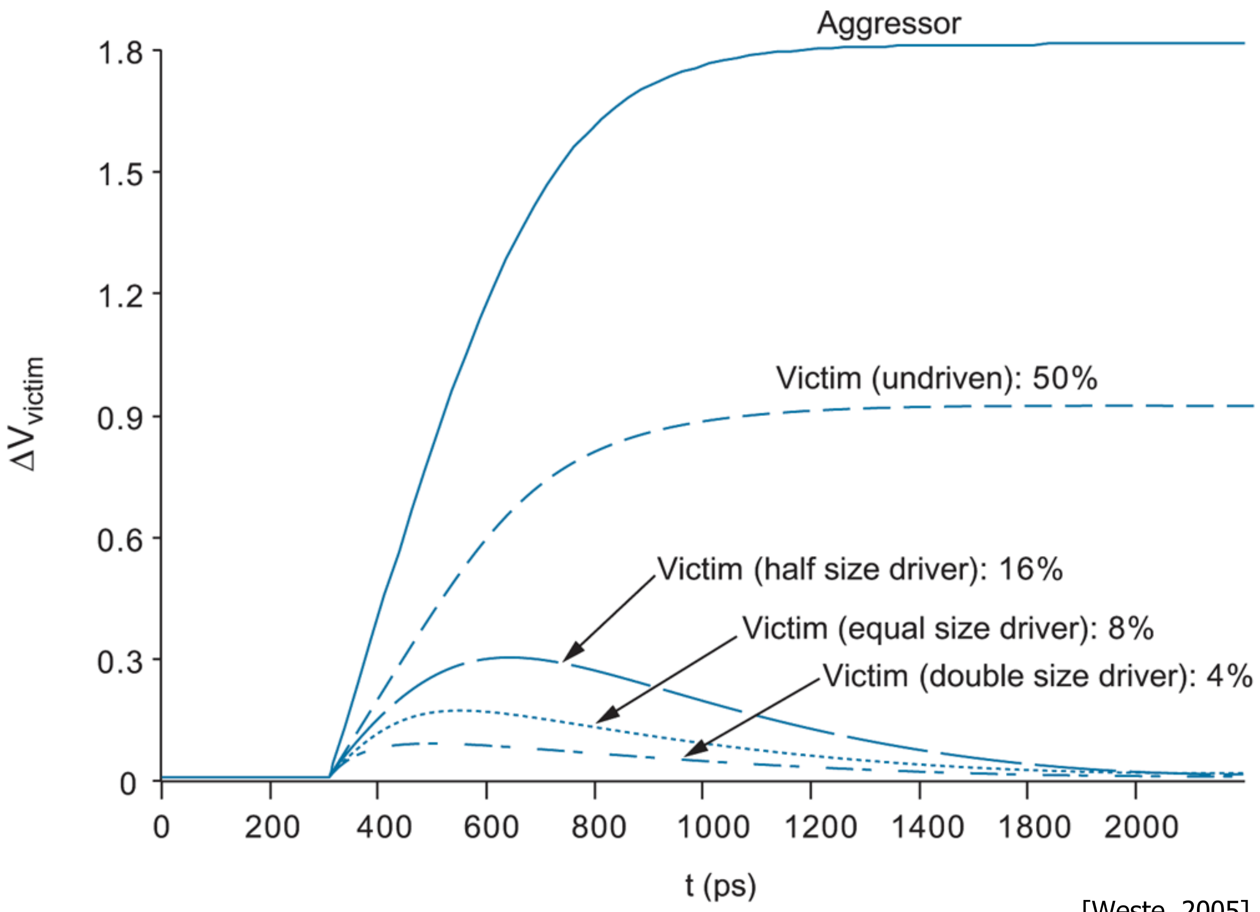
Further considerations

Effect of crosstalk



[Weste, 2005]

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Further considerations

- Inductance
- AC resistance

- Parameter variations

- Synchronization, latching
- Pipelining
- Handshaking

- Reliability
  - α-particles
  - Power supply noise
  - Substrate bounce

Outlook

Ongoing investigations / Open issues

- Routing schemes
- Topology
- Operating system (centralized)
  System control (distributed)
  - Power, temperature
  - Communication-computation trade-offs
  - Hardware reconfiguration
  - Self-healing, Reliability
  - Load balancing, task-mapping
  - Composability of functions/tasks/services
- Benchmarking