A Structural Architecture for HW Packet Processing

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Outline

- Packet Processing
- Architecture for Functional Modules
- Simulation Results
- A Packet Processor Architecture
- Conclusion

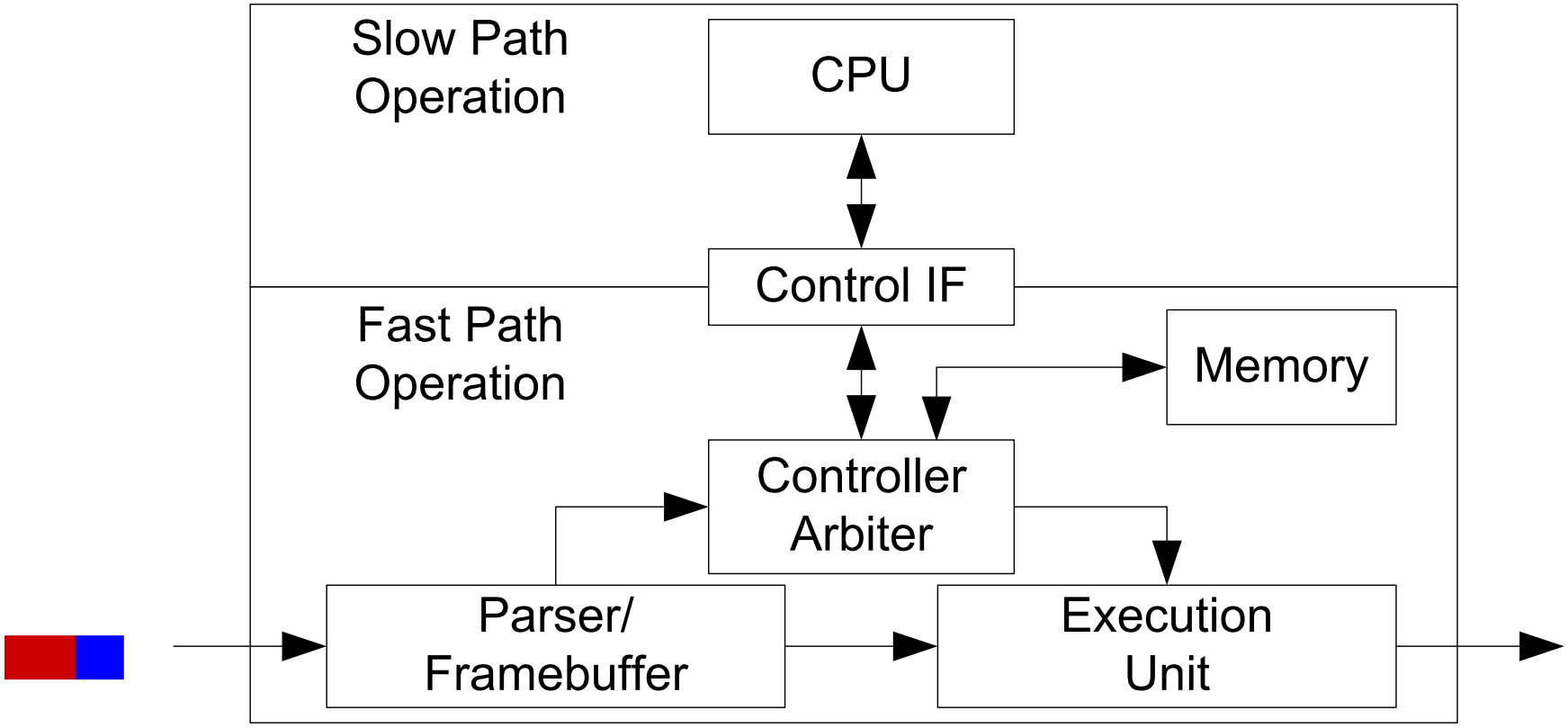
Packet Processing in Access Networks

- Various functionalities
- Highest speeds
- Highest throughput demands
- Software Solutions
  - + flexible, relatively cheap
  - - limited computational power and speed
- Hardware Solutions (ASICs)
  - + high speed
  - - inflexible, expensive
- FPGA – Solution
  - Flexibility of software solutions combined with the power of a hardware implementation

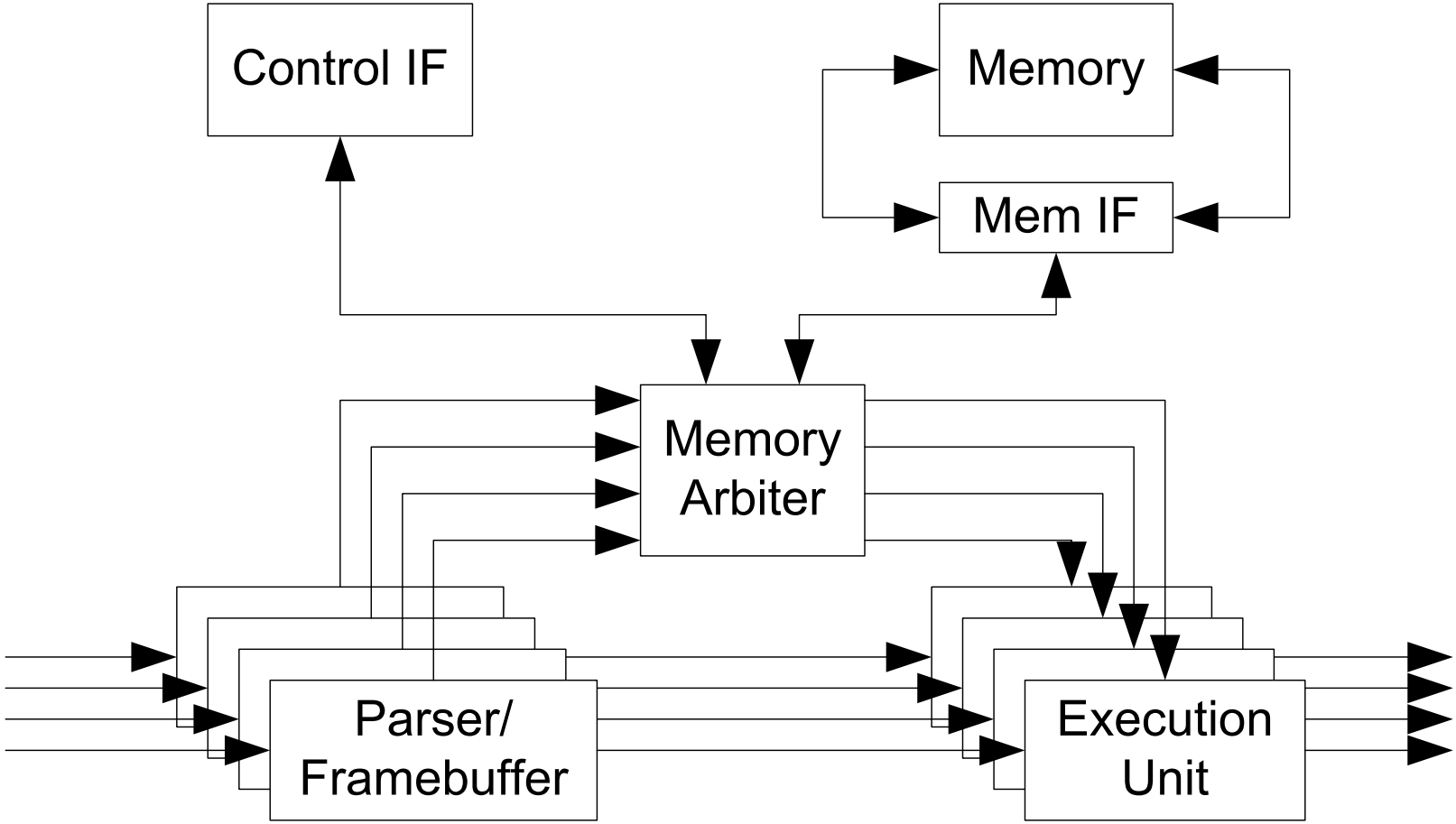
Packet Processing

- Slow Path → Low computational power
  - seldom
  - little relations to data path operations
- Fast Path → High computational power
  - Wire-speed
  - High throughput

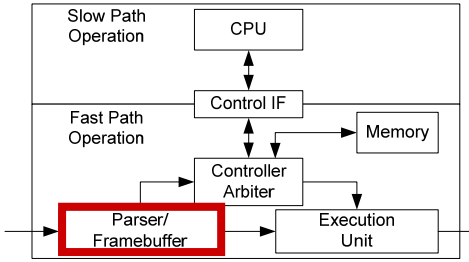
Packet Processing

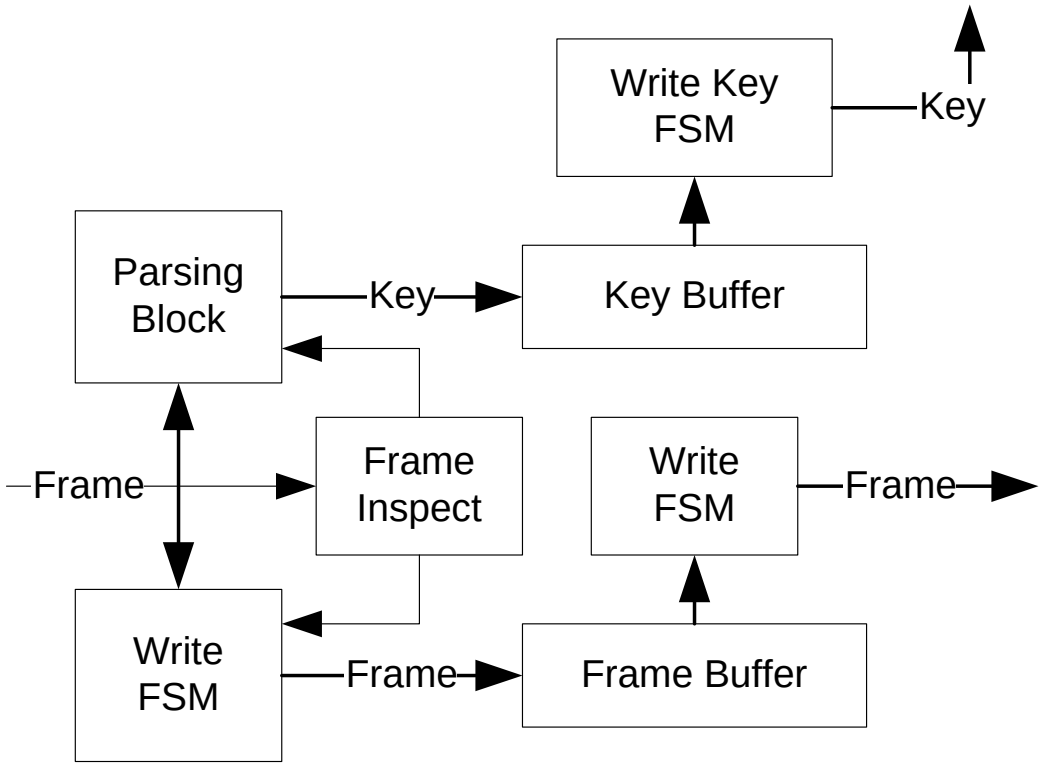


Functional Modules - Architecture



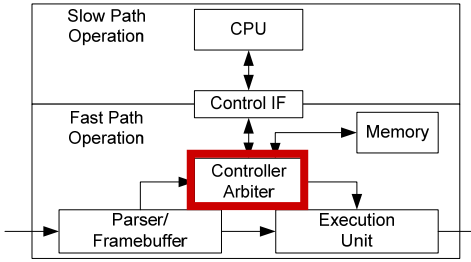
Parser & Framebuffer

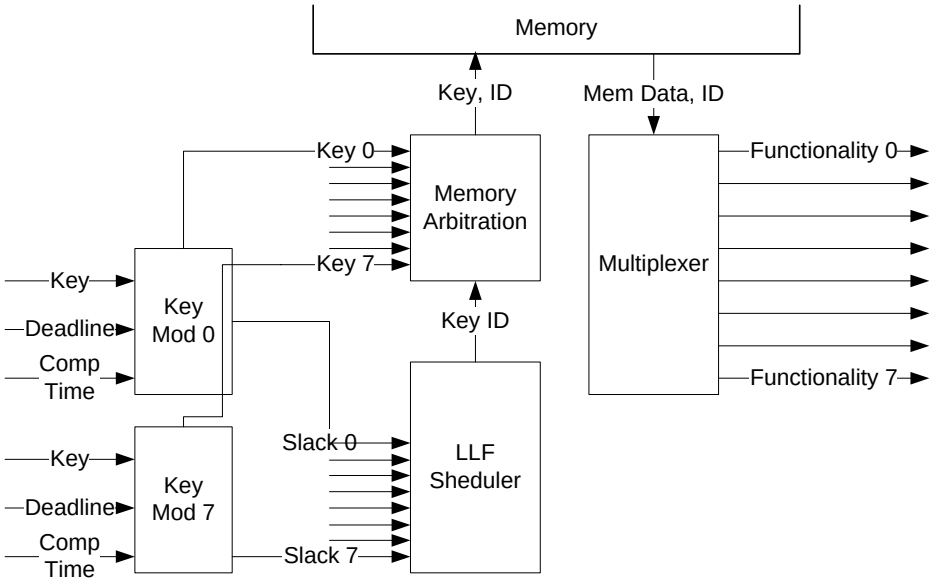




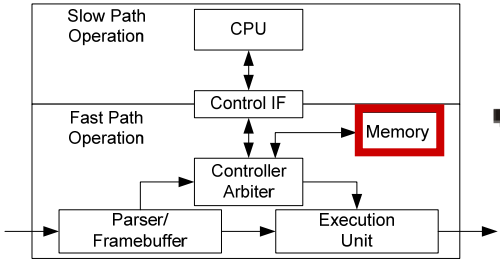
- Key Parsing
  - Configurable @ compilation time
  - For each header field instantiation of one parsing block
- Buffering of Frames
  - Whole Frame in the data path
  - Use of internal BRAMs
  - No external memory and off chip operations required

Memory Arbiter





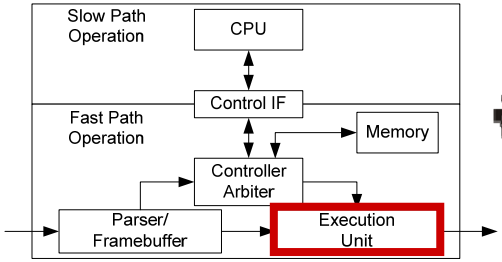
- Organization of communication within the FM
- Mainly memory arbiter functionality
- LLF scheduling for memory arbitration



Memory

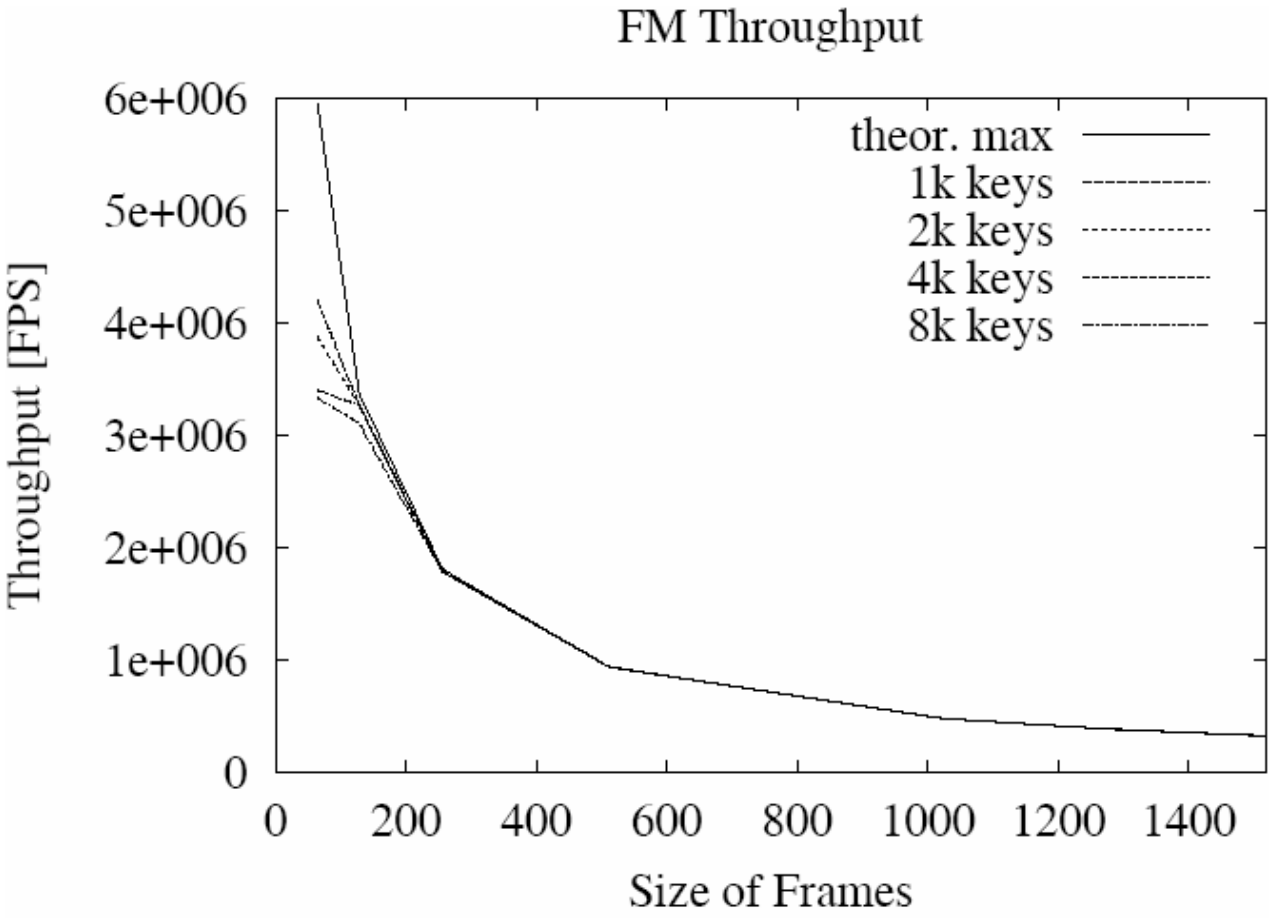
- Internal Block RAMs (BRAMs)
  - Limited capacity and high costs
  - Alternatively use of external SRAM
- Memory interface main bottleneck
  - Search: $O(\log_2(n))$
  - Insert/Delete: $O(n+\log_2(n))$
- Performance
  - 3 Gbit/s (minimal Frames)
  - 15 Gbit/s (realistic Frames)

Execution Units – Examples

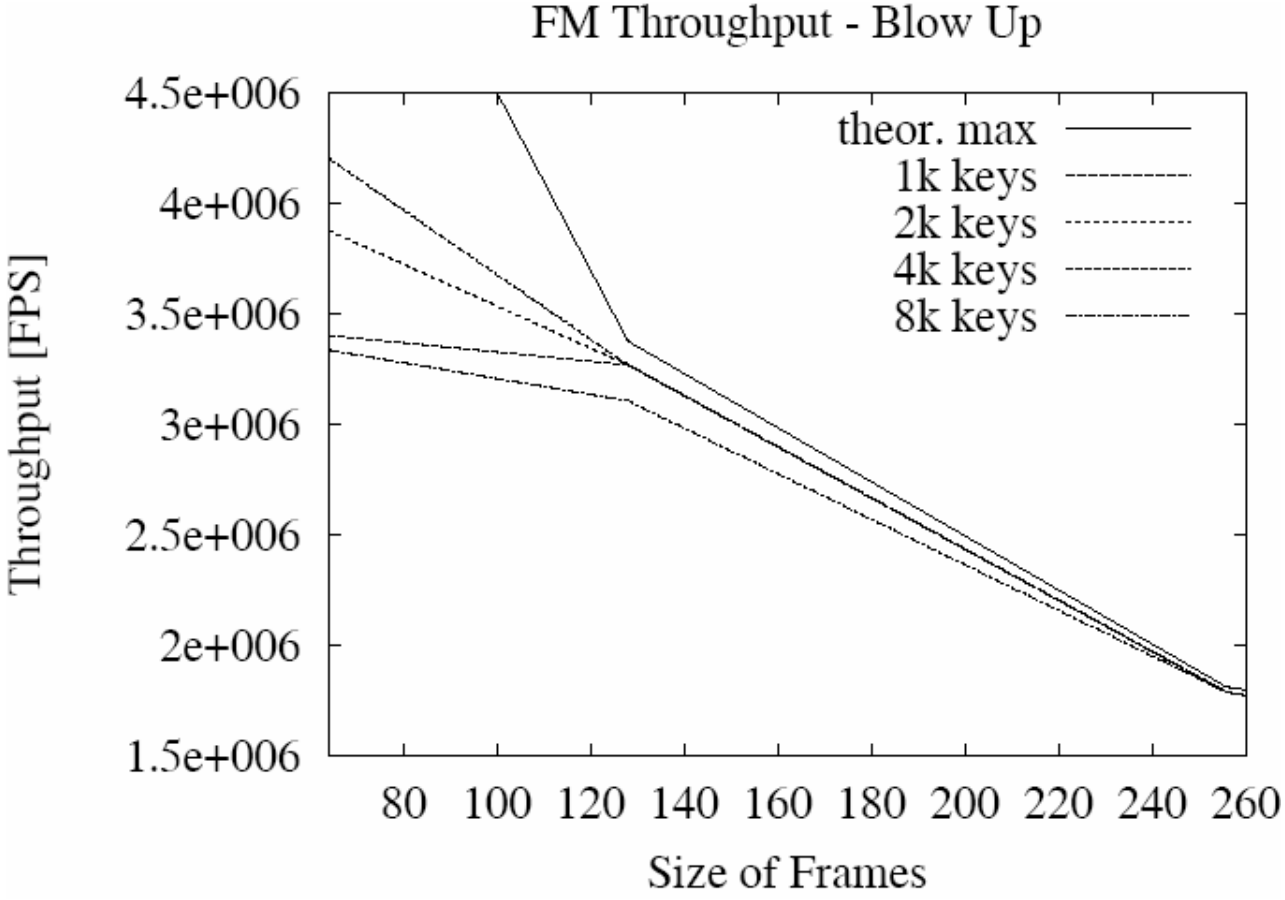


- MPLS-User Network Interface
  - Insert MPLS header into each incoming frame
- Mac Address Translation (MAT)
  - Replace customer's SRC-MAC with a network provided MAC
- Traffic Manager (TM)
  - Control the traffic of each customer within the Access Network and perform provisioning and color marking

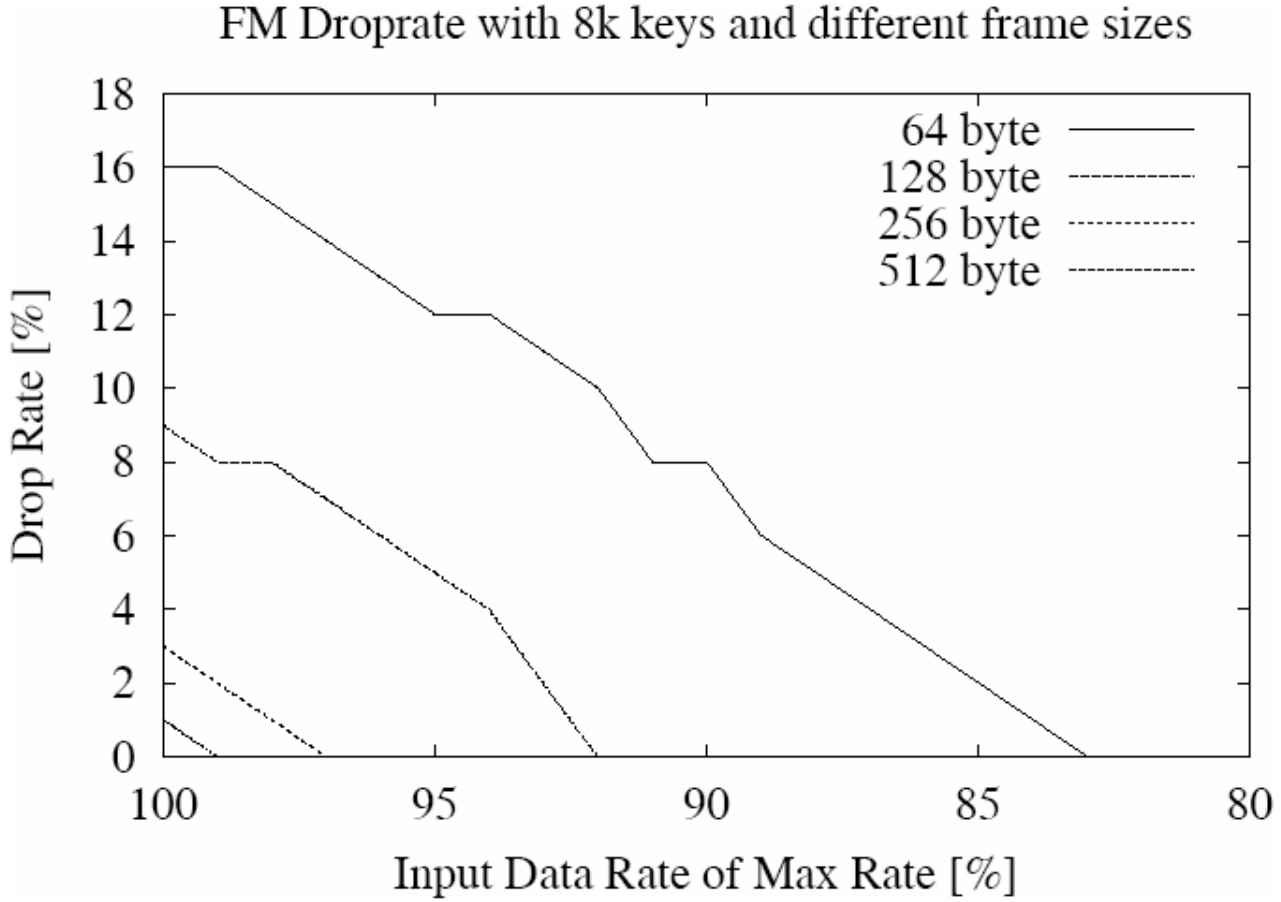
Performance – Throughput



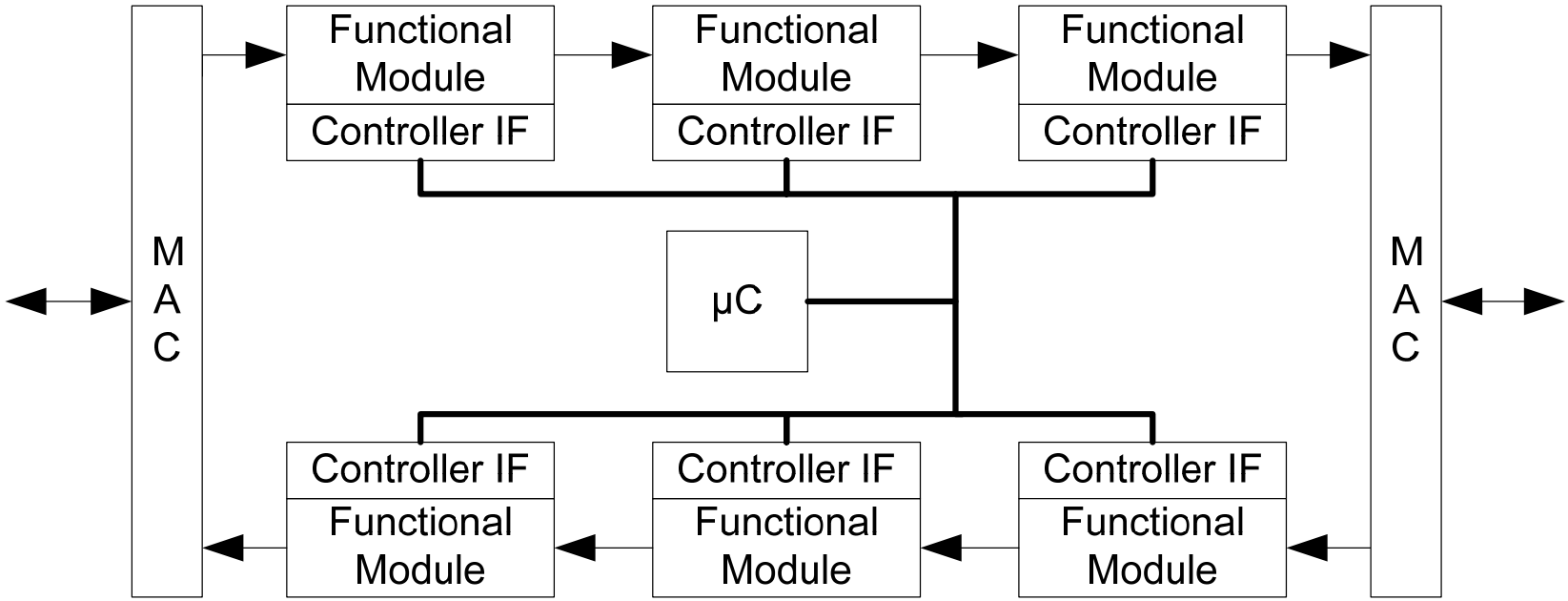
Performance – Throughput



Performance-Droprates



Packet Processor - Architecture



Conclusion & Outlook

- Architecture for packet processing elements with high performance and flexibility
- Functional Elements with 4 Gbit/s were developed and simulated
  - MPLS-UNI with 5000 Slices on V4FX20 FPGA
- Arrangement and interconnection of FEs on FPGA Platforms