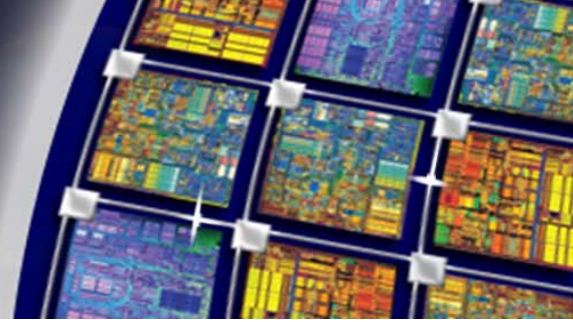


Trading hardware overhead for communication performance in mesh-type topologies

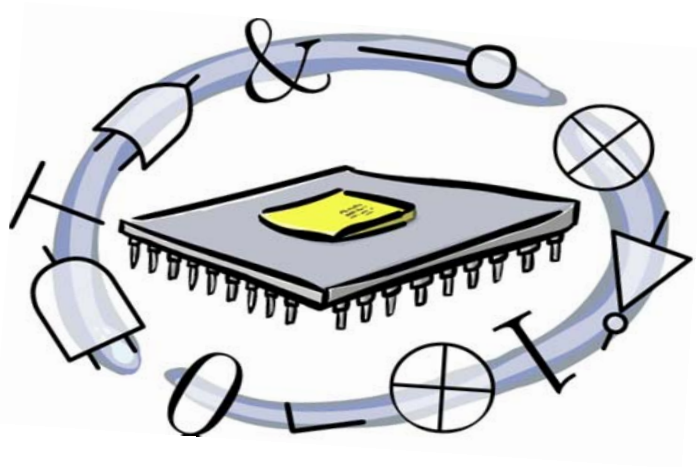
Claas Cornelius, Philipp Gorski, Stephan Kubisch, Dirk Timmermann

13th EUROMICRO Conference on Digital System Design (DSD)
- Architectures, Methods and Tools

University of Rostock
Institute of Applied Microelectronics and Computer Engineering

Outline

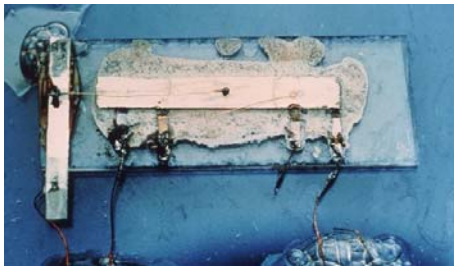
- Introduction
- Setup
  - Scenarios
  - BEAM – Border-Enhanced Mesh
- Discussion
  - Results
  - Open issues
- Conclusion



Introduction

Development of technology

- Continuous scaling of physical dimensions
  - Smaller devices
  - Higher integration density
  - Higher performance



1958: First IC

1981: Personal Computer (PC)

>2000: Functional integration

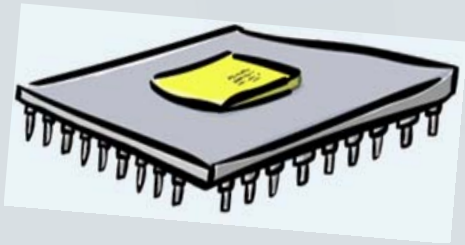
Introduction

Development of technology

- Continuous scaling of physical dimensions

Main challenges

- Productivity
- Power dissipation
- Reliability and robustness

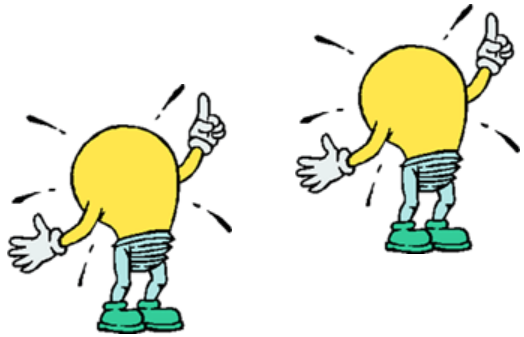


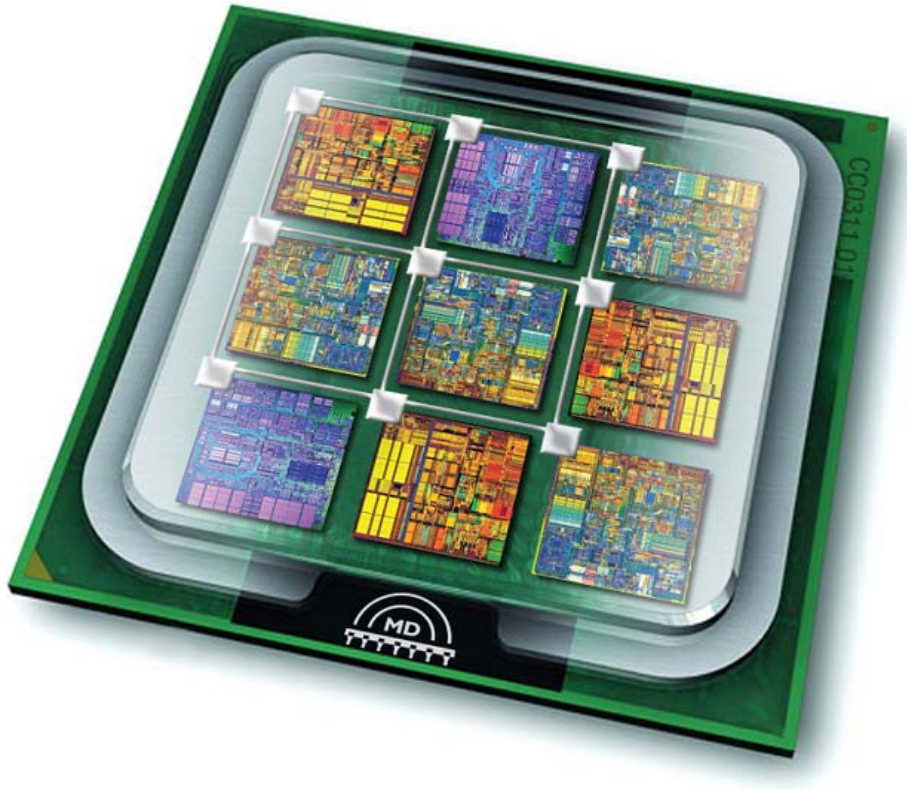
To cope with these challenges requires extensive research and development

Introduction

What shines brighter than a bulb?

Two bulbs





Key characteristics:

- **Parallelism**
- **Modularity**

Introduction

What shines brighter than a bulb?

Crucial change

Determining for efficiency becomes

- **Communication and**
- **Coordination**

Network-On-Chip (NOC) seems an appropriate design paradigm to cope with current concerns

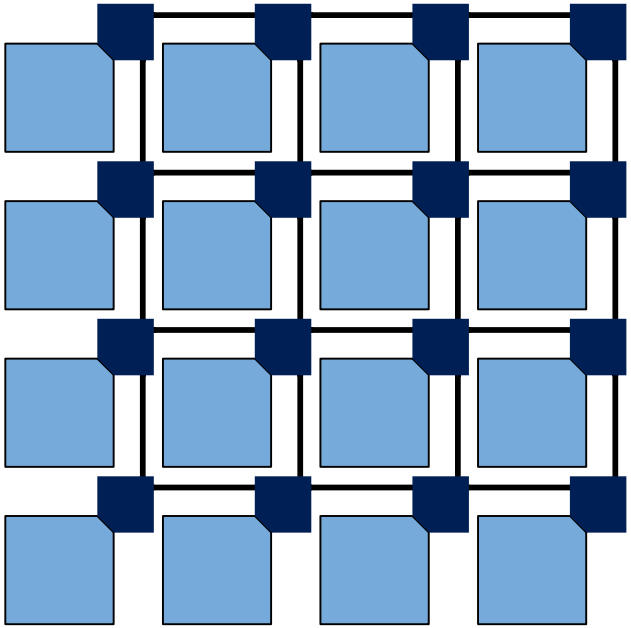
Setup

- **Selection of underlying platform**
  1. FPGA = Xilinx Virtex-4
     - Concerned with area usage
  2. ASIC = STMicroelectronics 65 nm
     - Concerned with power consumption

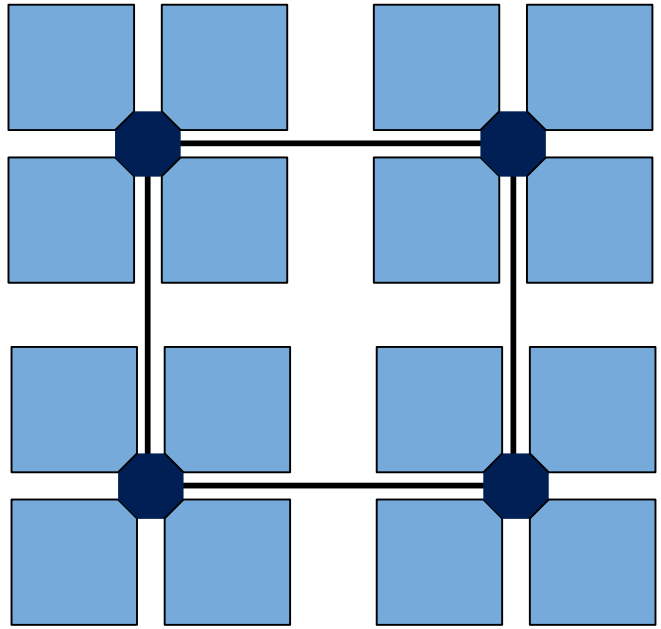
- **Application scenarios**
  1. Application-specific
     - Few heterogeneous resources
     - Known requirements
  2. Domain-specific
  3. General purpose:
     - Many homogeneous resources
     - Unknown requirements

Setup

Starting point: Mesh-type topologies



Standard mesh

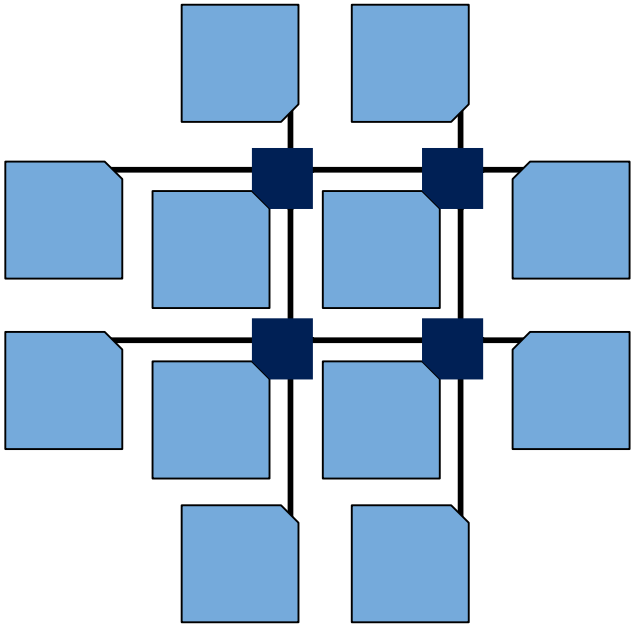


Concentrated mesh

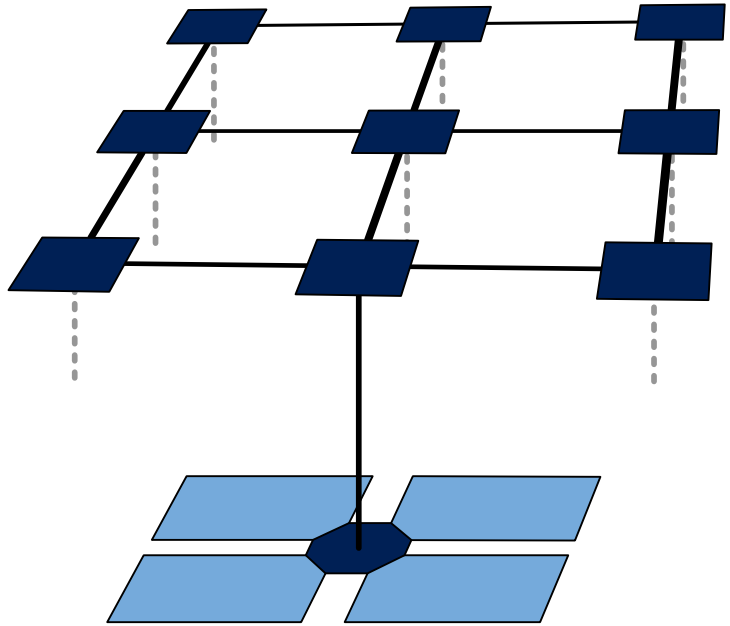
J. Balfour and W. Dally, “Design tradeoffs for tiled CMP on-chip networks,” In Proc. of ICS, 2006.

Setup

Starting point: Mesh-type topologies



BEAM



Clustered mesh

S. Bourduas and Z. Zilic, “A hybrid ring/mesh interconnect for network-on-chip using hierarchical rings for global routing,” In Proc. of NOCS, 2007.

Setup – BEAM

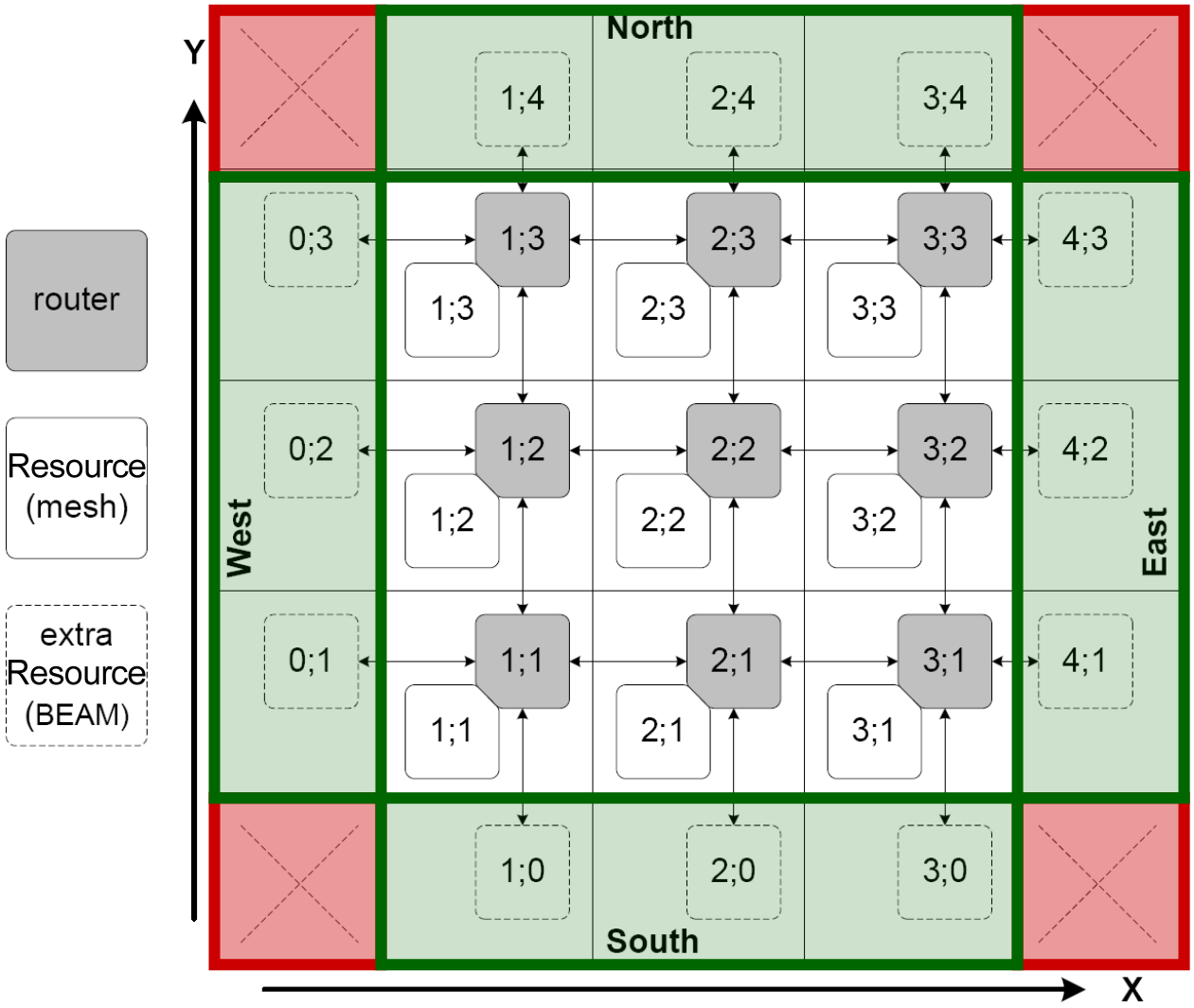
Border-Enhanced Mesh (BEAM)

- Key objectives:
  - Reduced overall overhead
  - Maintaining regularity
  - Use of only low-radix routers *
  - Cartesian addressing
  - Dimension-ordered routing

* A. Ferrante, S. Medardoni, and D. Bertozzi, “Network interface sharing techniques for area optimized NoC architectures,” In Proc. of DSD, 2008.

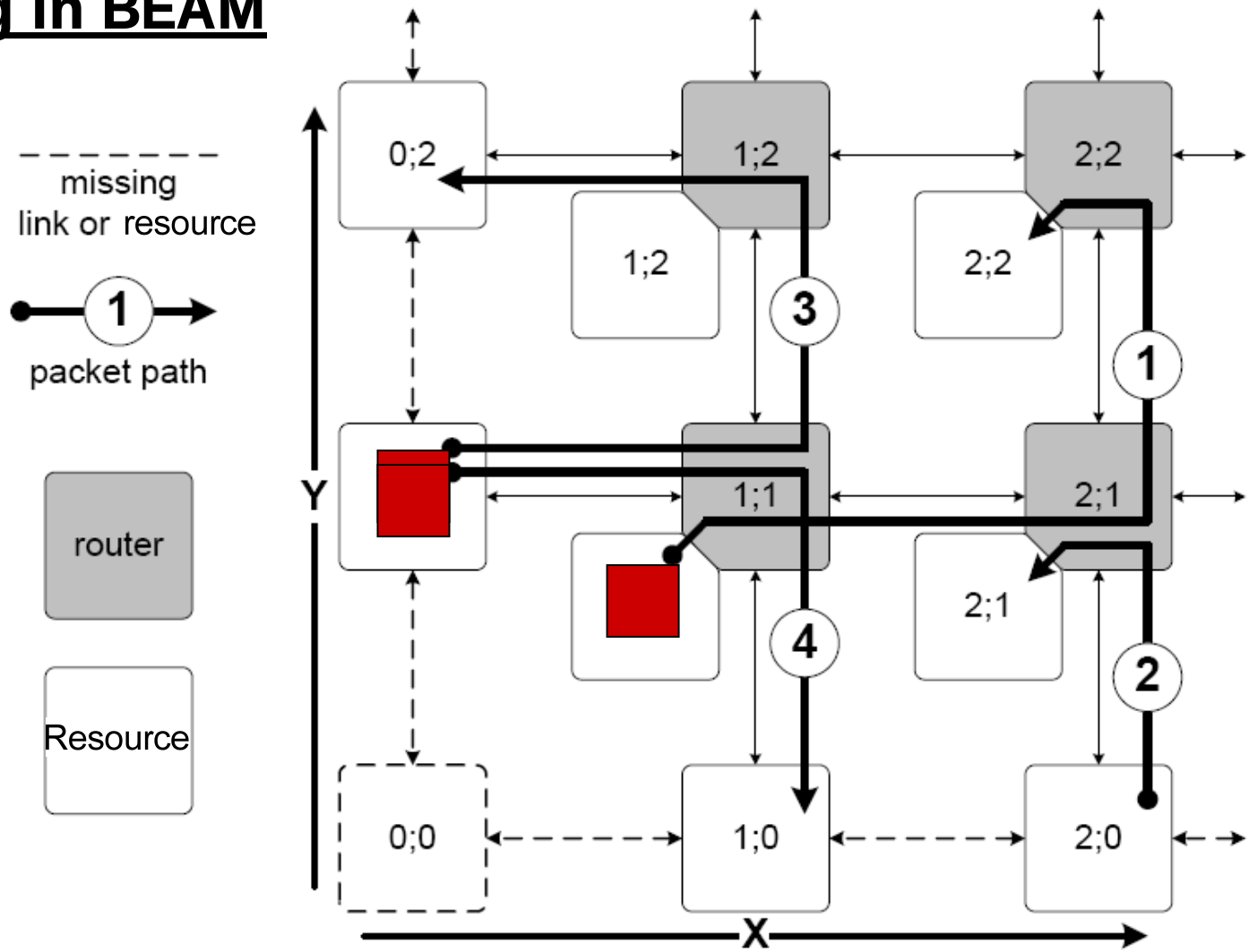
Setup – BEAM

Topology and its addressing



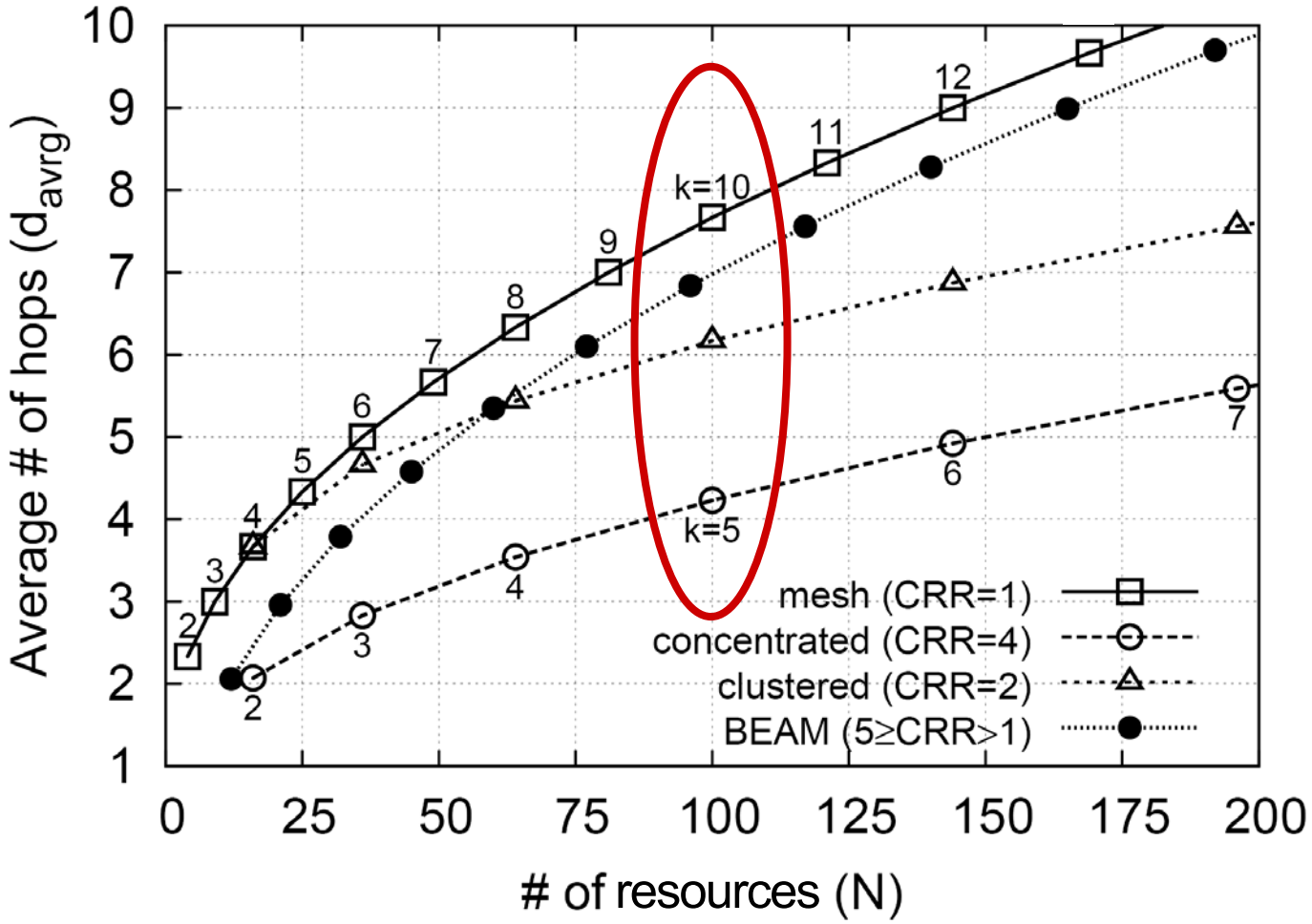
Setup – BEAM

Routing in BEAM



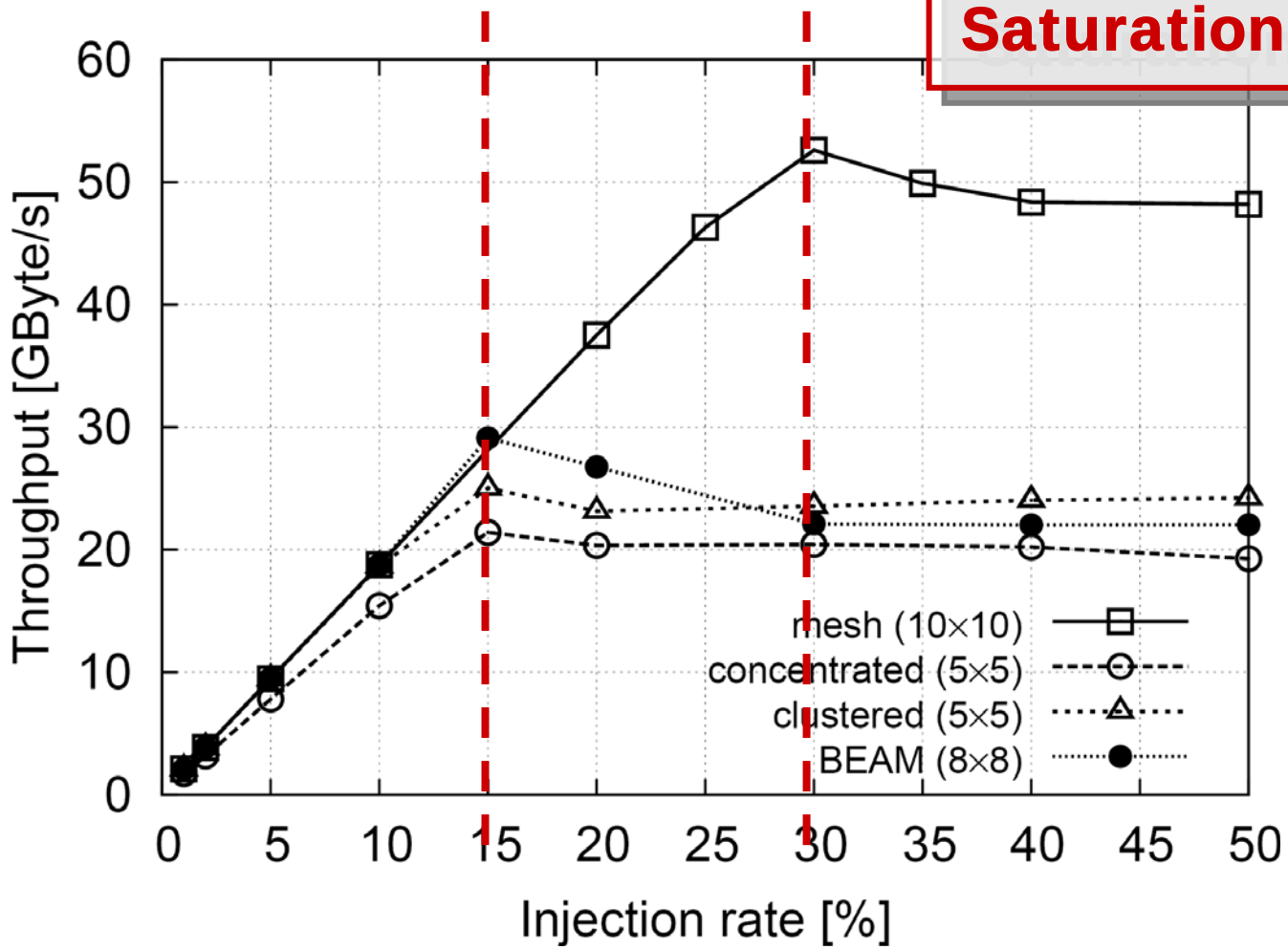
Results

Analytical comparison



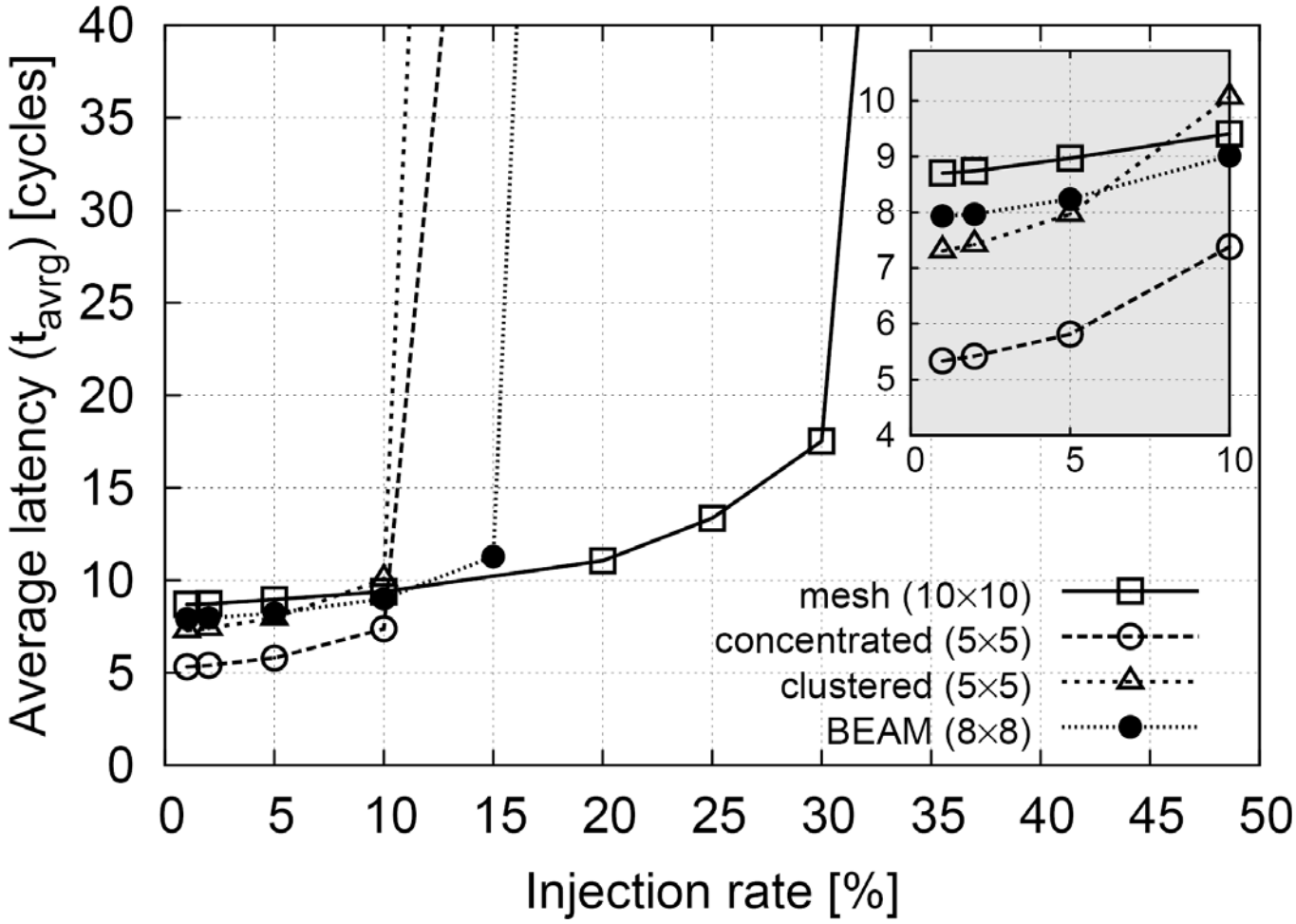
Results

Communication characteristics I



Results

Communication characteristics II



Results

Synthesis

- Number of routers only a first measure
- Higher radix hurts the frequency

	FPGA		ASIC		
type	slices	f [MHz]	power	area	f [MHz]
mesh	100 %	126,8	100 %	100 %	900,1
concentrated	55,24 %	110,2	32,56 %	40,74 %	740,8
clustered	51,40 %	118,5	49,82 %	51,52 %	897,5
BEAM	66,06 %	131,4	72,74 %	72,79 %	939,4

Open issues

Benchmarking

- Setup influences results drastically, consider
  - Packet lengths, traffic patterns
  - Presented metrics
- Necessary benchmark suites have to be
  - platform-dependent and
  - domain-specific.

Comparison of solutions and results becomes questionable without accepted measures.

C. Grecu, et al., “Towards open network-on-chip benchmarks,” In Proc. of NOCS, 2007.

E. Salminen, et al., “Requirements for network-on-chip benchmarking,” In Proc. of NORCHIP, 2005.

Open issues

Reliability and robustness

- Complex systems will exhibit failures
  - But most contributions on NOC assume faultless operation

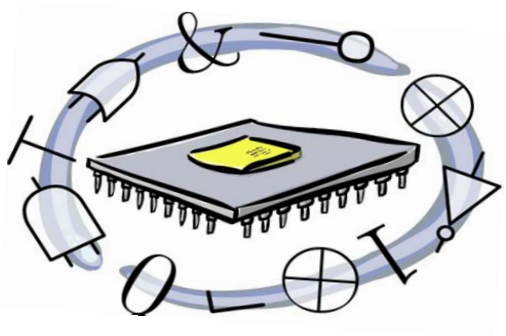
- To be answered (an extract):
  - **Physical** = Which causes to consider?
  - **Models** = How to integrate models into the design process?
  - **Metrics** = How to evaluate reliability and robustness?

- Suggestion: **Energy-Reliability Ratio (ERR)**

$$\mathrm{ERR} = \frac{P_{\mathrm{tot}} \cdot t_{\mathrm{d}}}{\mathrm{Reliability}} = \frac{\mathrm{Energy}}{\mathrm{Reliability}}$$

Conclusion

- Mesh-type topologies are beneficial for the use in complex Networks-On-Chip (NOC)
- Comparison of different mesh-type topologies
- Selection of best suited topology highly depends on given requirements
  - Characteristics have to be traded off



- Open concerns that restrain further research on NOC
  - Accepted benchmark suites are required
  - Reliability has to be considered as a key design quality