

# Temperature and On-chip Crosstalk Measurement using Ring Oscillators in FPGA

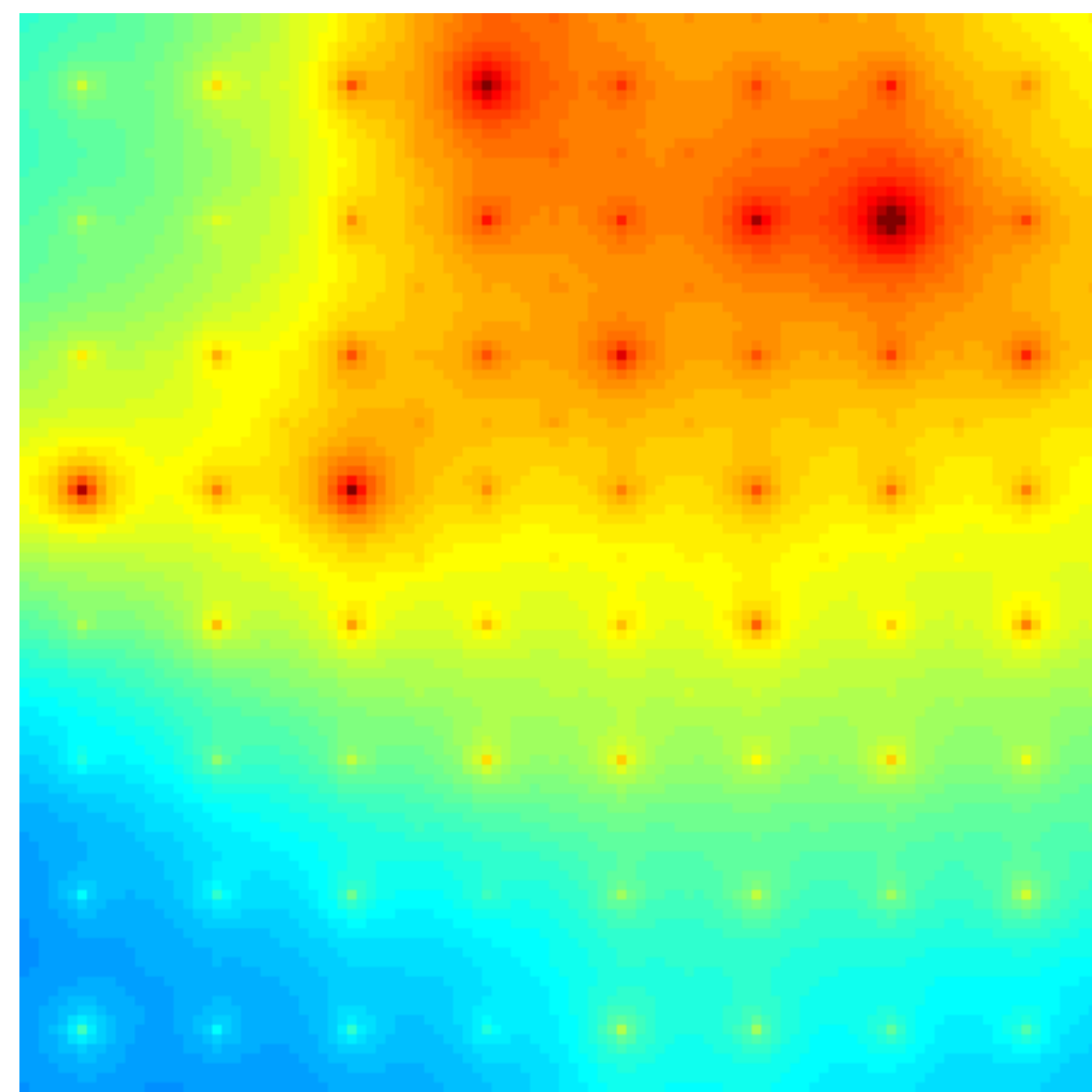
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## Motivation

- Power density ↑
- Process variations ↑
- Heterogeneous Systems-on-Chip

### Thermal Imbalances

- Thermal Monitoring
  - Need small distributed sensors
  - Compile temperature map
  - Enable thermal management

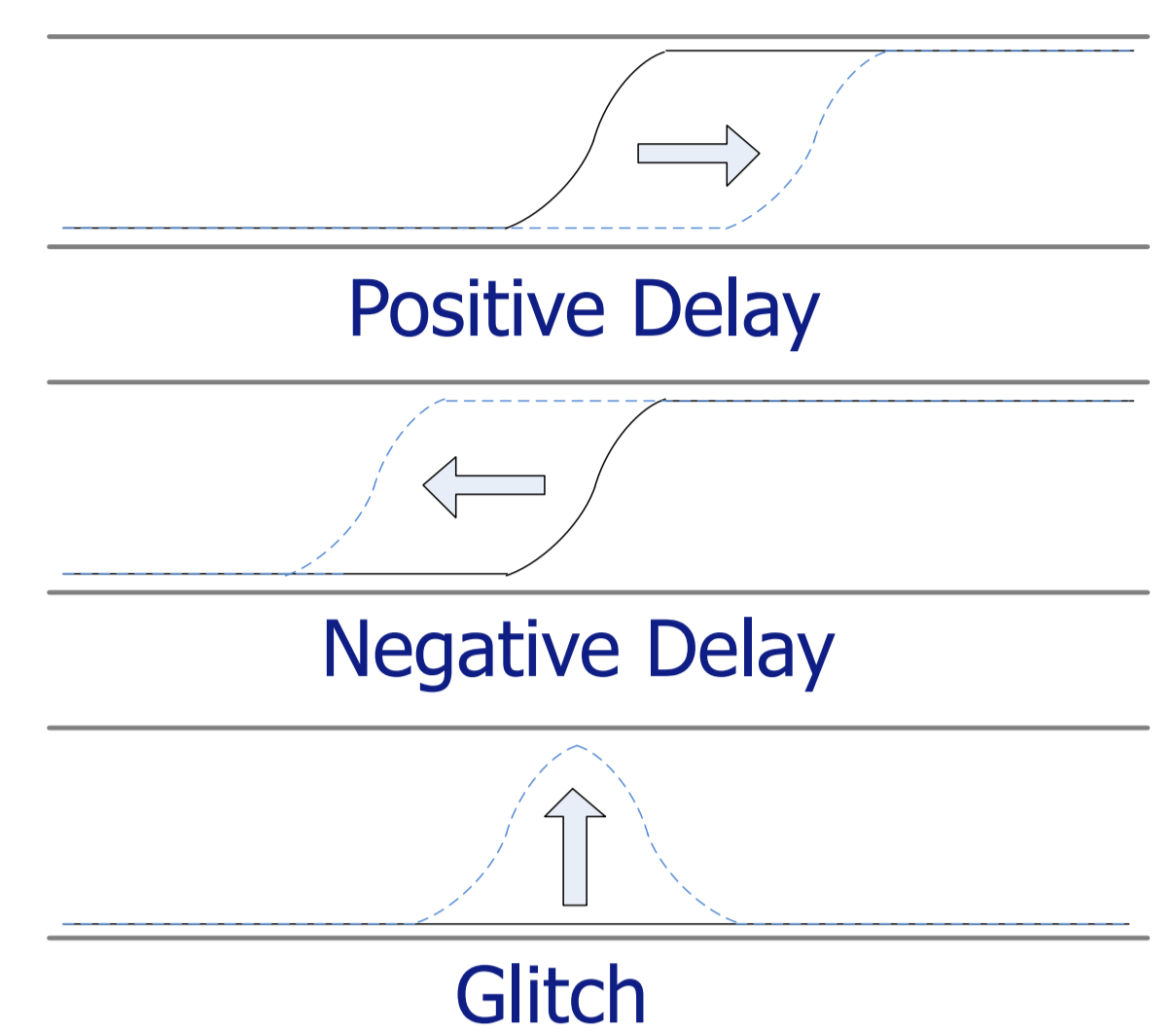


- Computational resources ↑
- Communicational resources →
- Capacitances ↑
- Variations ↑

### Signal Integrity and Aging

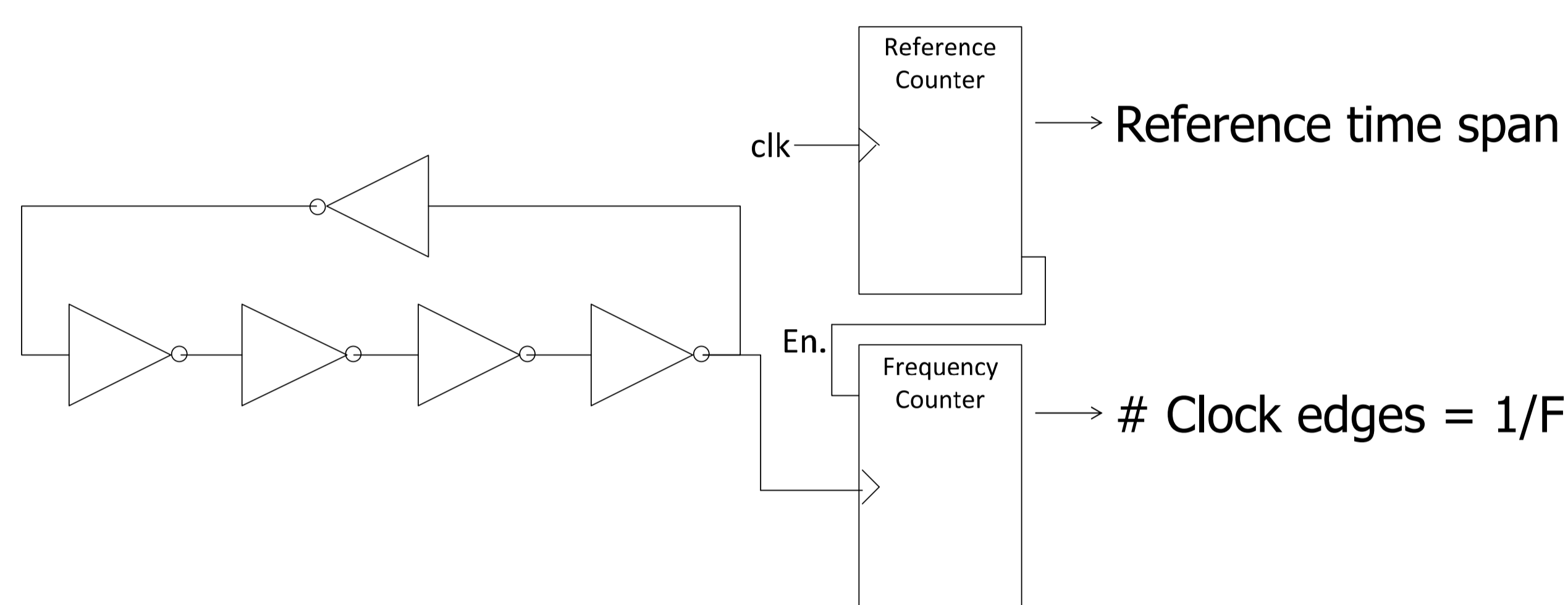
- Need to sense delay
- + Coupling induced delay
- Test circuit on FPGA

Crosstalk induced phenomena:



## Measurement of On-chip Temperature and Crosstalk

Temperature sensitive ring oscillator with frequency counter:

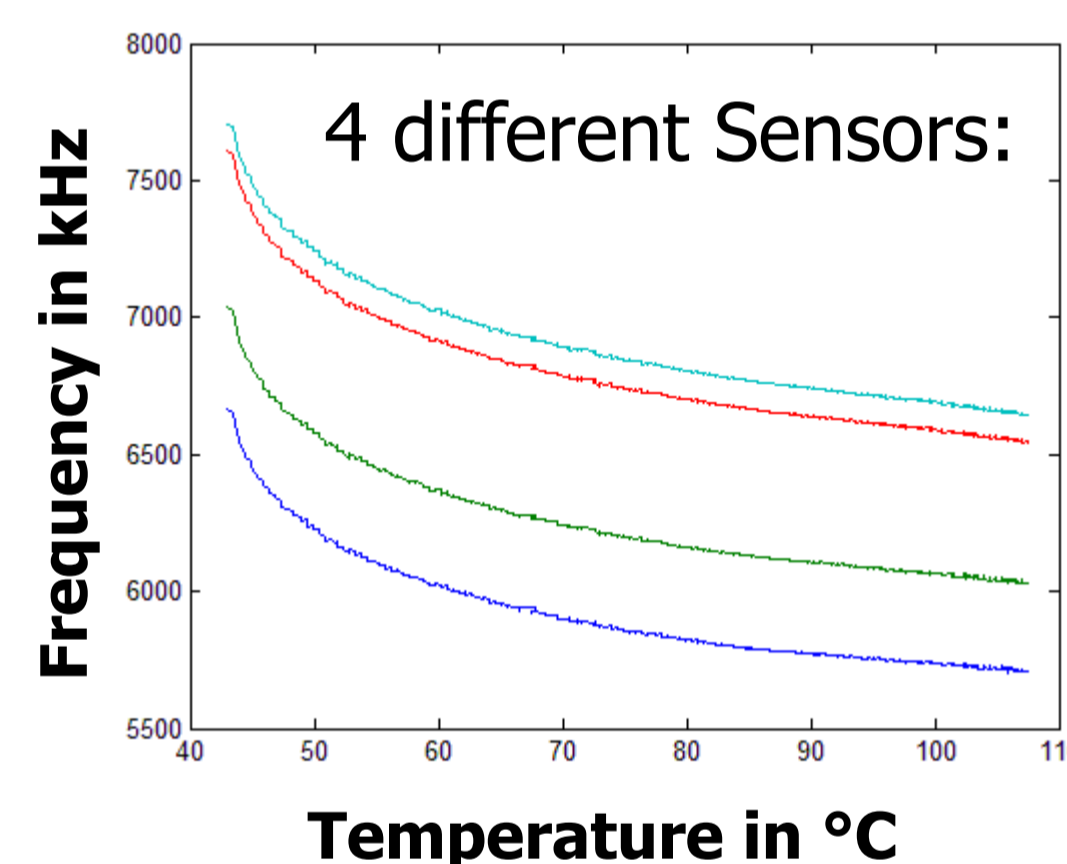


Frequency depends on supply voltage and temperature

$$V_t = V_{t0} + \alpha_{V_t} \cdot (T - T_0)$$

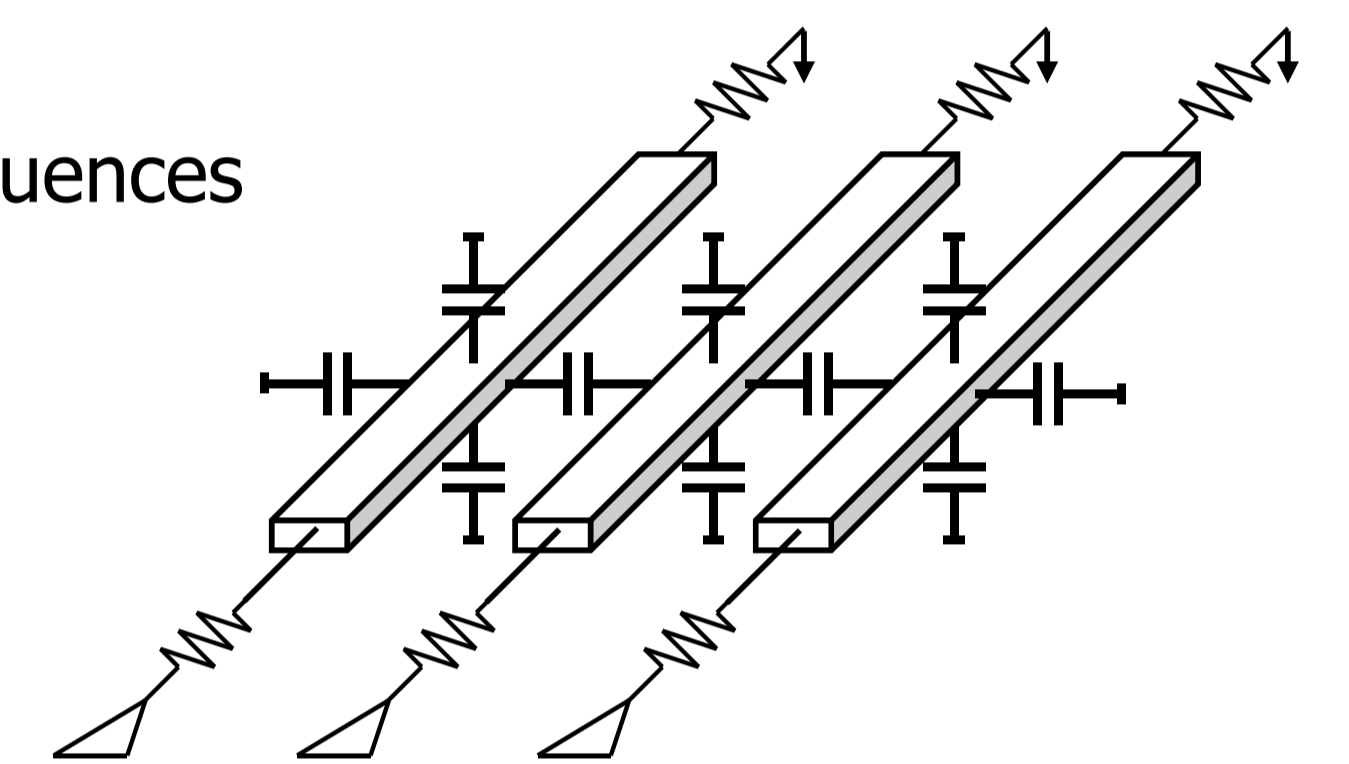
for  $\alpha_{V_t} = -2 \dots -4 \left[ \frac{mV}{K} \right]$

$$\mu = \mu_0 \cdot \left( \frac{T}{T_0} \right)^{\alpha_\mu} \text{ for } \alpha_\mu = -1.5 \dots -2.5$$



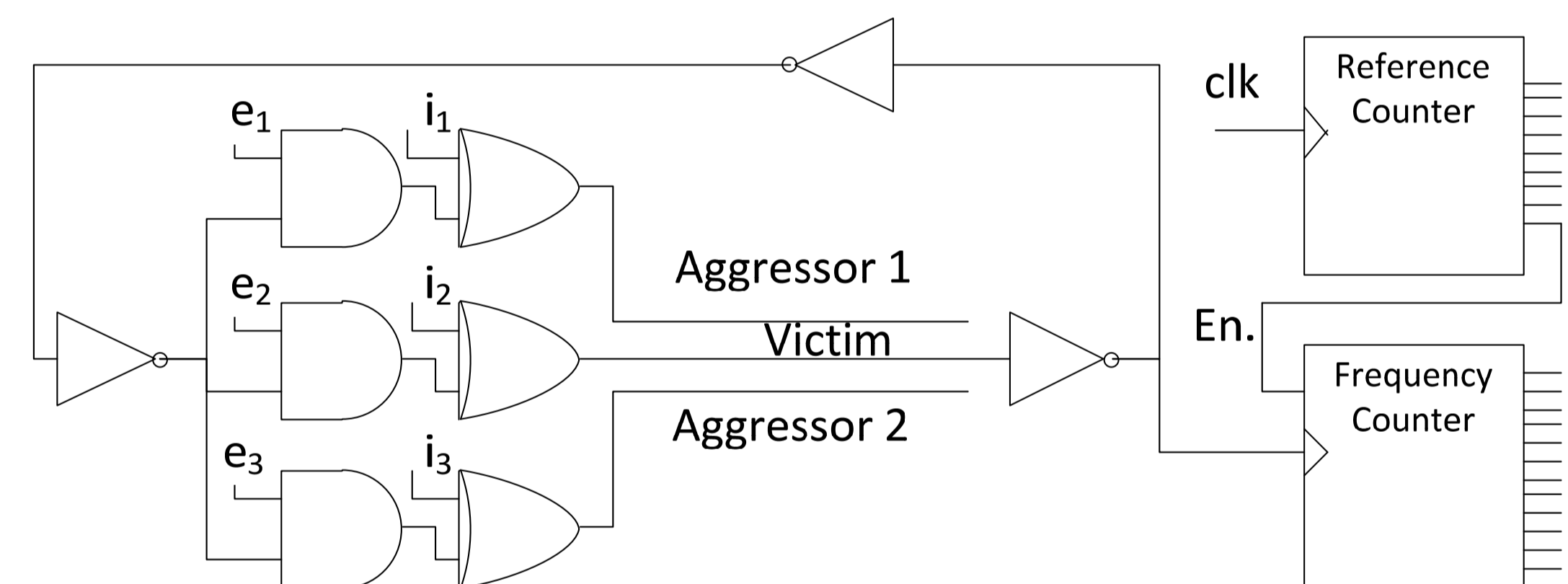
- Influence of  $\mu$  is dominating
- Overall a linear relationship is assumed
- Only true for certain temperatures:

- Capacitive coupling
- Activity on neighboring wires influences voltage level
- Induced delay can be positive or negative



Ring oscillator for measuring coupling induced delay:

- Contains test line (victim) and
- Neighboring aggressors

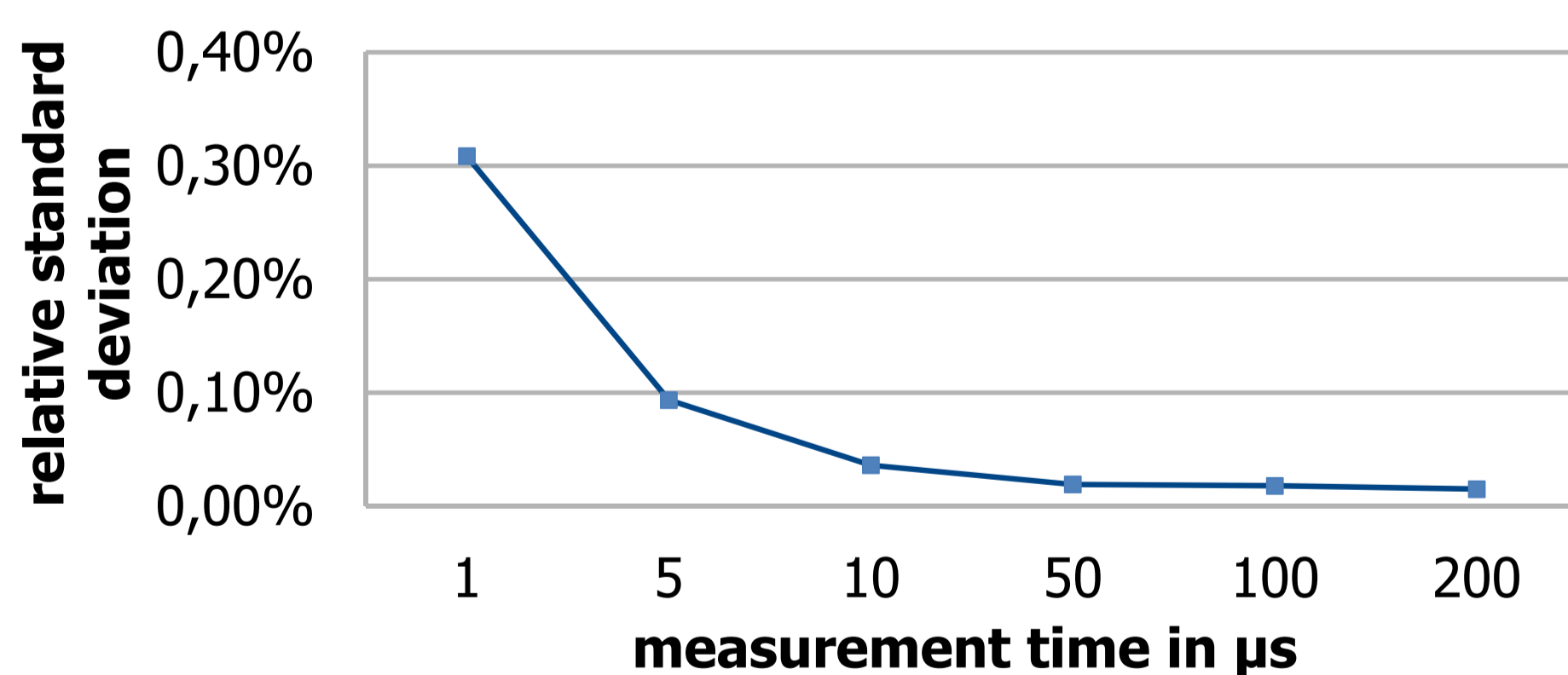


Inputs e and i allow to create all possible crosstalk patterns  
 → Change of frequency

Precision depending on parameters like:

- Ring length,
- Measurement time, ...

Best parameter set -> ~0.012%

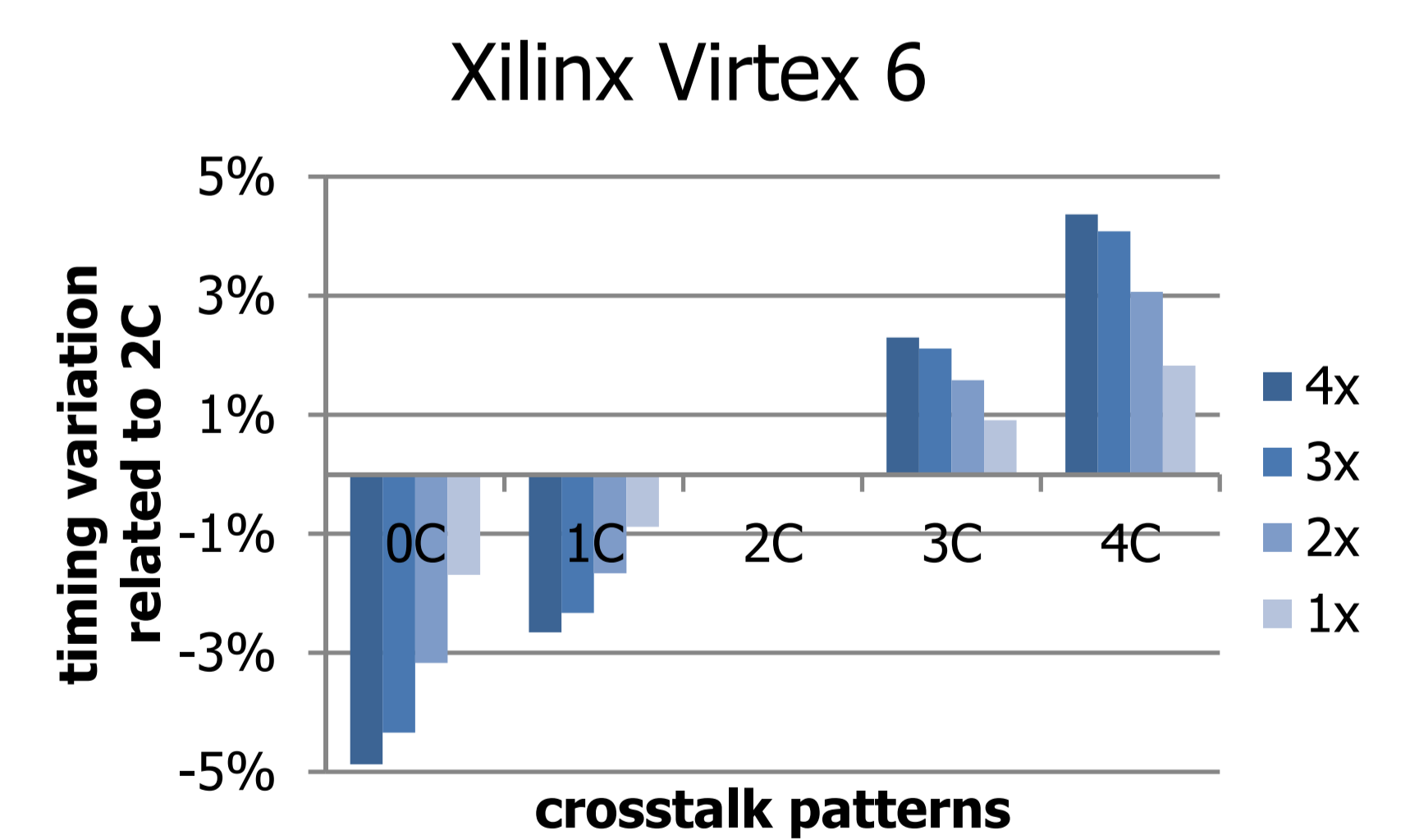
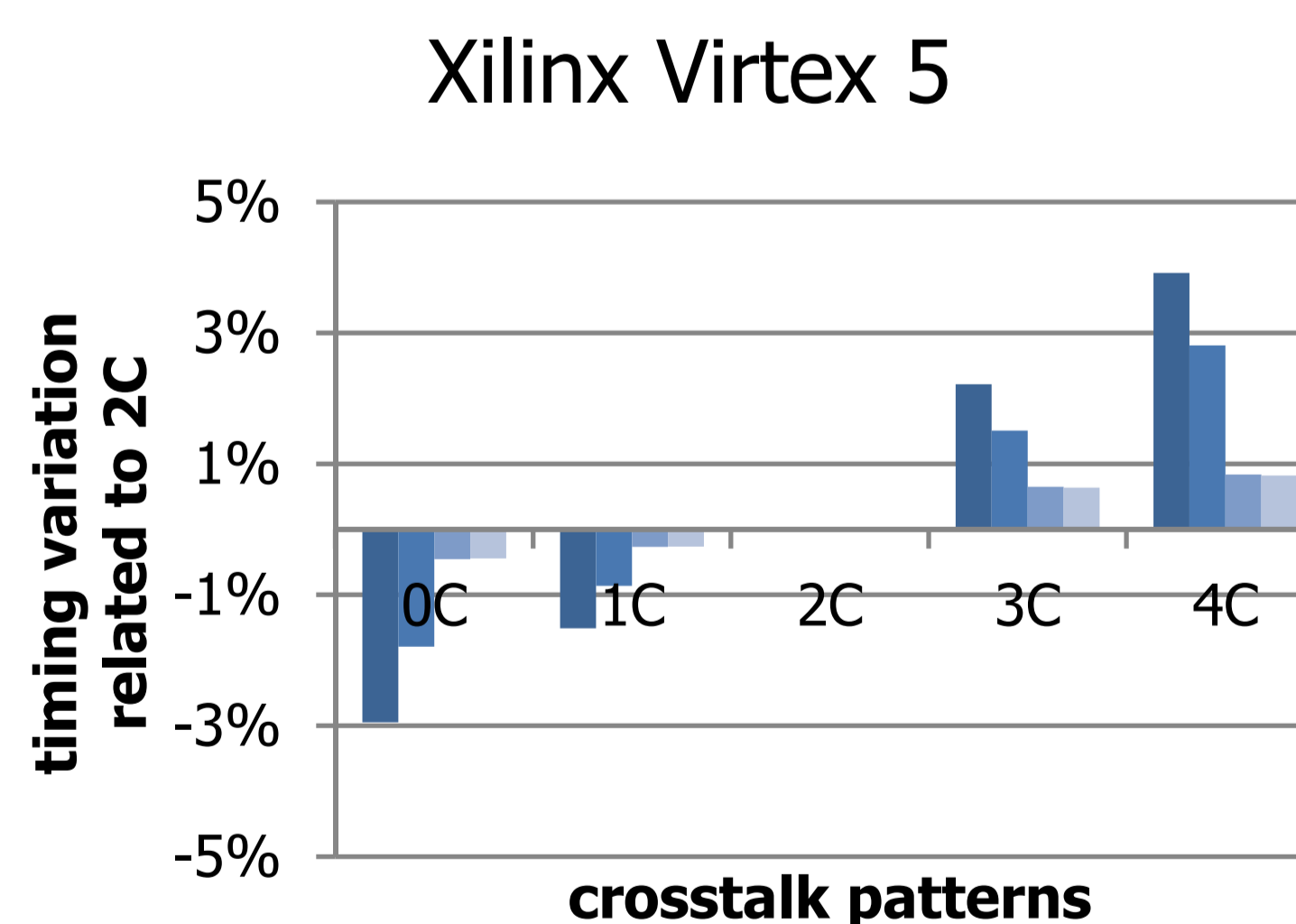


Scattering an array of sensors is possible  
 Calibration of multiple sensors could be tricky

→ Runtime Thermal Management,  
 Temperature Aware Mapping,  
 ...

## Results of Measurements

Coupling induced delay is measured  
 All crosstalk patterns can be differentiated



Very small standard error: 0,0001%

Measured over different wire length: 4x = ~ 1/4 chip length -> up to 9% delay variation  
 2x = ~ 1/8 chip length, ...

→ Higher influence of crosstalk on Virtex 6 (40 nm) than on Virtex 5 (65 nm)

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