

Applications Session

Data Flow Based System Level Design and Analysis of Concurrent Image Processing Applications

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Abstract

In order to escape the complexity trap of modern embedded systems, many new design methodologies emerge which promise to ease system design by hiding implementation details. However, due to Turing complete specifications, system level analysis and optimization typically restricts to simulation techniques or is not possible at all.

In order to solve these difficulties, *SystemCoDesigner* has been proposed, which permits for high level system description using precise models of computation. In particular it is one of the first approaches that unifies both multi-dimensional and one-dimensional data flow in order to describe concurrent hardware-software systems. Integration of a finite state machine responsible for communication control permits to describe and classify both static and dynamic algorithms. This not only helps to design complex image processing applications containing data dependent decisions like entropy decoding, but also supports for efficient representation of regular algorithms like the discrete cosine transform or data reordering. This leads to several benefits. First of all, efficient system level analysis like polyhedral scheduling or buffer analysis is able to dimension the memory sizes required for throughput-optimized execution of the static multidimensional application parts. Secondly, an automatic design space exploration supports the designer in selecting the appropriate implementation alternative for each data flow actor. This includes both hardware-software partitioning as well as the decision which implementation alternative of a required hardware accelerator shall be employed. This is possible by means of a multi-objective evolutionary optimization that targets minimization of the required hardware resources and maximization of the achievable throughput. The latter is evaluated by a fine-grained architectural simulation in order to deliver accurate results in presence of data dependent decisions.

The system architecture resulting from the automatic design space exploration can then be automatically synthesized. Whereas the different data flow actors can be generated by means of different behavioral compilers, a novel communication synthesis approach is able to automatically deliver high-speed communication primitives for multi-dimensional communication. They offer very high clock frequencies and throughput that is sufficient for real-time processing of images with cinema resolution. Furthermore, different implementation alternatives can be automatically generated from the same application specification, which permits to trade required hardware resources against attainable throughput. Compared to solutions obtained by behavioral synthesis of one-dimensional actor models, this leads to faster implementations requiring less hardware resources as demonstrated by means of a Motion-JPEG decoder.

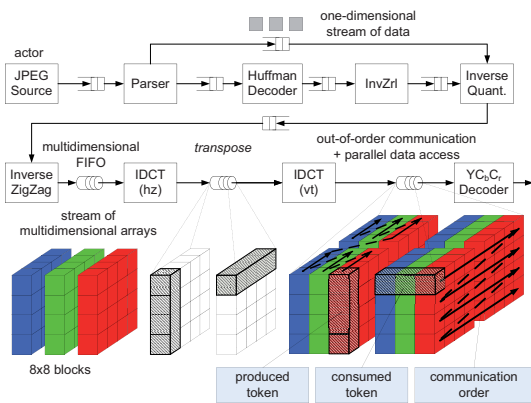
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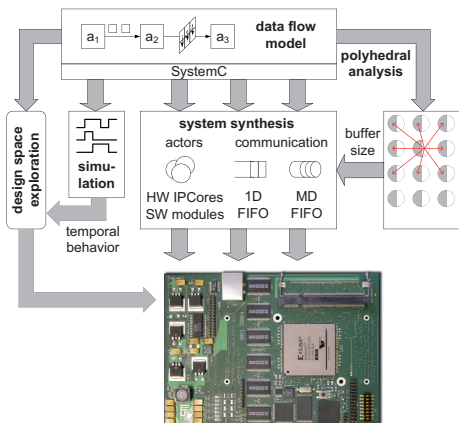
Motivation

- Image processing applications operate on **both one-dimensional and multidimensional streams** of data
- Include **regular static** algorithms (IDCT, YCbCr decoder) and **data dependent** operations (Huffman Decoder, InvZrl)

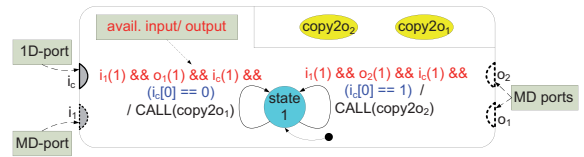


- Complexity requires new design methodologies that offer a higher level of abstraction
- Well known approaches such as SystemC or Simulink are restricted to one-dimensional streams of data
- Multidimensional methodologies are still in their infancy
- Proposition of a novel design methodology that **unifies both one- and multidimensional data flow**
- Combines the advantages of data flow based design with polyhedral analysis and synthesis
 - Block-diagram-like system specification
 - Efficient system level analysis such as automatic buffer size determination
 - Synthesis of high-speed communication primitives and actors

SystemCoDesigner Flow

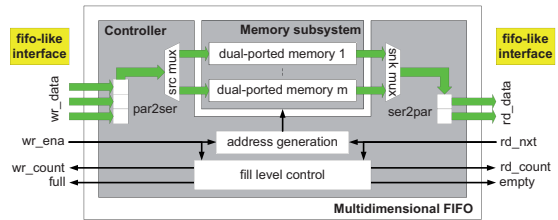


Structured Actor Specification in SystemC



- **Ports** can be connected to one- and multidimensional FIFOs
- **Finite state machine** controls communication
- Flow control by checking availability of input tokens/windows and free space for output tokens
- Data dependency by **guards**
- Permits **classification** of static and data-dependent algorithms

Communication Synthesis



- **FIFO-like interface** for simple system integration
- **Automatic generation** from data flow specification by static compile-time analysis in order to reduce run-time overhead
- Parameterized with read and write orders
- Tracks the current read and write position
- Provision of a memory subsystem that allows to **read and write several data elements per clock cycle**
- Parallel to serial conversion allows **trading throughput against required hardware resources**
- **High clock frequencies** (up to **400Mhz** for a Virtex4 FPGA) by pipelining
- Sufficient for real-time processing of images in digital cinema resolution
- Permits for **faster communication with less resources** compared to behavioral synthesis of one-dimensional actors

