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Design Space Exploration for Distributed Hardware Reconfigurable Systems*

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A recent trend towards networked and hardware reconfigurable systems can be identified in several areas like automotive, ambient intelligence, and many more. On the other hand, there is a lack of sophisticated design automation tools which support designers during the design process. With the increasing complexity of such modern embedded systems, an urgent need for design tools at higher levels of abstraction can be seen. The most challenging tasks in system-level design for networked reconfigurable systems is to guarantee the feasibility of solutions while exploring giant design spaces. To overcome these problems, a hierarchical graph-based model for networked hardware reconfigurable systems is introduced. The hierarchical system model consists of three parts: (i) A hierarchical process graph modeling the desired functionality of the system. Subgraphs associated with processes are used as alternative refinements for these processes. (ii) A hierarchical architecture graph representing the set of allocatable platforms. Subgraphs associated with hardware components are meant to be alternative configurations of hardware reconfigurable components. (iii) Hierarchical mapping edges relate processes with components of the architecture graph in a sense that these processes may be executed on the associated hardware components. The novelty of this model lies in the ability to support (i) Platform-based design: By optimizing a platform not only for a single static process graph but for a set of different refinements. (ii) Reconfigurable computing systems: The hierarchical architecture graph allows to exchange hardware functionality at runtime. (iii) Modeling of IP cores: Hierarchical mapping edges model partial implementations or subsystems with unknown properties. In contrast to existing solutions which mostly assume implicit communication between configurations and where configurations are constructed by structural temporal partitioning, our model is a real system-level model based on functional partitioning, since it supports explicit communication which let us detect hidden deadlocks in an implementation and configurations consist of system-level components like CPU, IP cores, buses, or even again FPGAs. In this Ph.D.-program, different methods for accelerating the task of design space exploration by exploiting the hierarchical structure of the underlying model have been proposed. All these approaches are based on Evolutionary Optimization. The most outstanding idea is called Pareto-Front Arithmetics where subsystems are optimized independently of each other. Later, the optimization results are combined regarding the hierarchical problem structure. Moreover, new formal methods based on SAT-techniques for testing the feasibility of an implementation have been developed. Furthermore, these SAT-techniques can be extended towards an analysis strategy to determine the degree of fault tolerance of a networked hardware reconfigurable system. The feasibility of this work, was shown by developing a networked hardware reconfigurable system, called ReCoNet.

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